VLSI DESIGN METHODOLOGY
THE PROBLEM OF THE 80'S FOR MICROPROCESSOR DESIGN

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ABSTRACT

The rapid evolution of semiconductor technology continues to make possible increasingly sophisticated electronic systems on single chips of silicon. By 1982, a single silicon chip is projected to have well over 100,000 transistors. This level of complexity represents a major problem for the VLSI designer in the 1980's. Unless there is a major change in design methodology, this level of VLSI technology will be grossly under-utilized due to the problems of design, layout and checking. With present design methods, a 100,000 transistor MOS chip will take 60 man years to layout and another 60 man years to debug.

INTRODUCTION

At present design rates, it is clear that the major problem for the 1980's will be to devise new design methodology in order that our rapidly evolving semiconductor technology, with all its density, will be widely usable by the electronics community. While technology has increased the on-chip complexity by a factor of four in the last two years, present designs are still based on methods that have not changed in the last six or seven years. This means, of course, that it now takes that much more of a manufacturer's resources to design each chip. In addition to the resources, the time to design, debug and transfer a complex microprocessor to production has increased at the same rate.

Clearly, the next challenge for manufacturers of VLSI devices will be how to reduce the resources and the time from conception to volume production of complex microprocessor chip families. While there are many aspects of this problem, which will require new methodology, this paper will focus on just one of these -- the portion of the design cycle known as "layout". This is the most expensive and time consuming portion of the design cycle and the one needing the most attention.

GROWTH IN COMPLEXITY

By using the number of active transistors on a chip as a general measure of complexity and by plotting it against the year of introduction of that microprocessor, one can begin to understand the magnitude of the problem.

Figure 1 shows the historical density improvement for microprocessor technology. Notice that the complexity of microprocessors at the chip level has grown exponentially for the last few years. This ever increasing number of devices on a chip will continue to make the layout portion of the design cycle the largest cost and time component. It could even be stated that the layout will become the dominant factor in development cost, and possibly, the limiting factor in chip design.

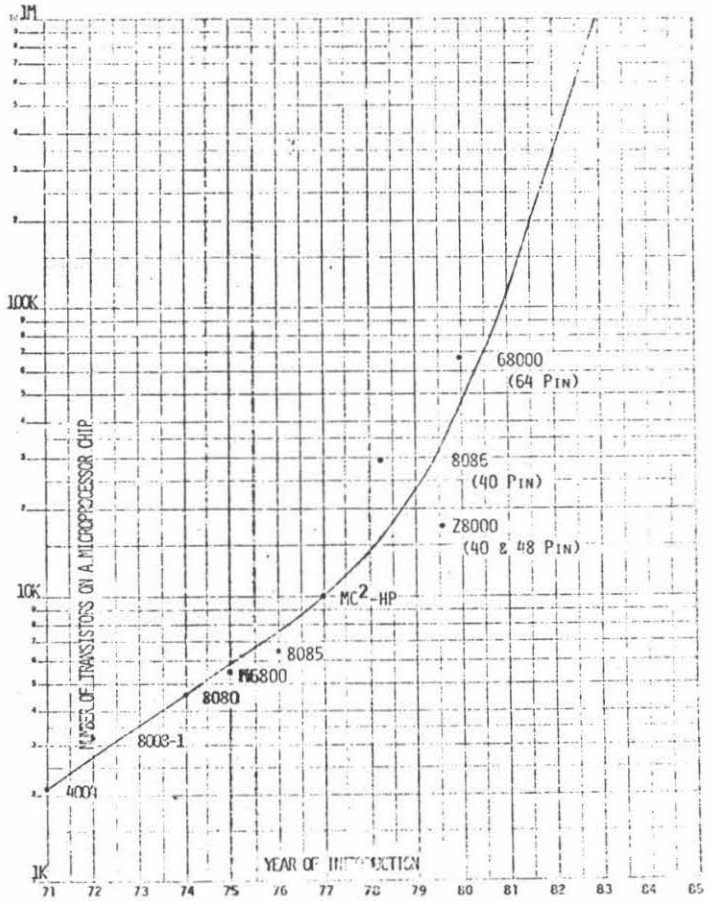

Figure 1

PRODUCTIVITY

Over the last few years, layout productivity has decreased as chip complexity has increased. This productivity, for a wide variety of layout techniques, including interactive drawing systems, is between five and ten devices per layout designer per day. This includes the time to draw, check and correct a layout.

If one assumes some productivity figure, a chart of estimated manpower can be derived from Figure 1. Figure 2 is such a chart and is derived from Figure 1 by using the number of transistors provided by the technology and translating that into man years of layout effort. The figure assumes that each layout designer can achieve the optimistic productivity level of ten transistors per day. The graph shows that a complex microprocessor in 1982 will take over 60 man years to layout. Since that level of layout effort would be almost impossible to manage, it means that the technology will have outrun the semiconductor manufacturer's ability to use it in a timely manner -- at least for complex logic chips.

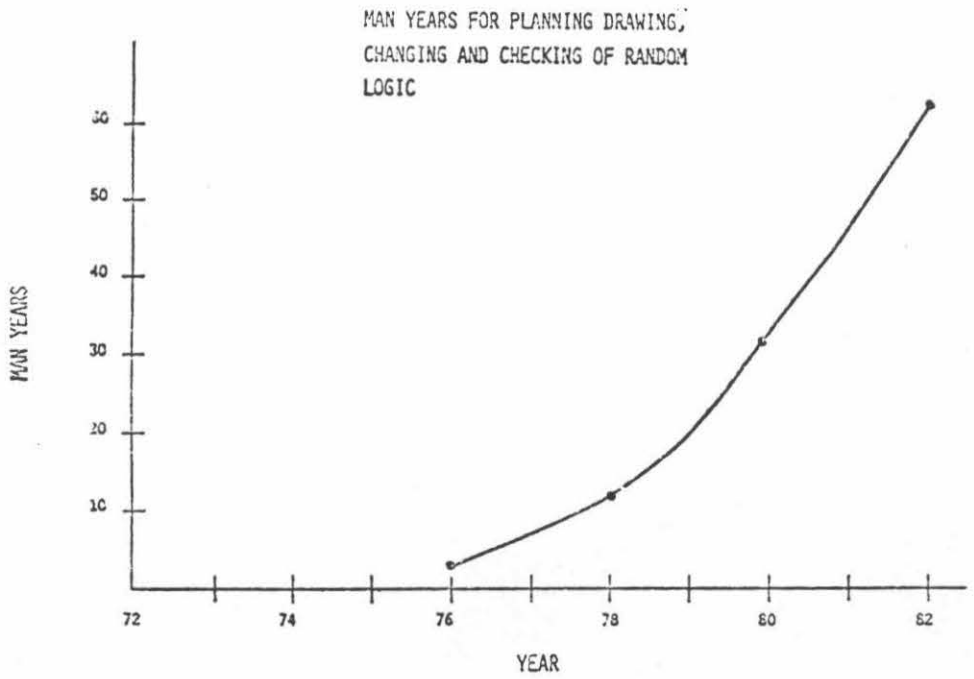

Figure 2

REGULARIZED STRUCTURES

It is important to note that Figure 2 does not apply to memory chips in that time frame since their layout is based on the design of a single cell which can be layed out once and then replicated many times automatically.

A similar concept has been proposed by Sutherland and Mead (Ref. 1) as a method to keep logic chip complexity from becoming unwieldy. It is a concept whereby random logic layout with its massive interconnection problems is structured by a set of well defined communication paths. These structures are usually implemented with very regular cells such as ROM's, RAM's and PLA's; although it is the geometric regularity of the interconnection between elements that provides the greatest benefit in reducing complexity. This paper would suggest a second major benefit of designing complex microprocessors with regular structures, and that is a decrease in layout time and effort. This decrease comes about because the use of regular structures reduces the total number of devices which must be individually drawn. In addition, the more structured layouts are easier to validate and check out.

To assess the impact of regular structures on layout time, we need a way to measure the degree of regularization on a given chip. The following parameter provides us with such a measure:

$$\text{Chip Regularization} = \frac{\text{Total Devices On A Chip}}{\text{Drawn Devices}}$$

where total devices includes all possible ROM and PLA placements, not just the bits actually programmed. The drawn devices are the devices that must be drawn, and therefore, require layout effort. This simple parameter matches an intuitive feel as to the degree of regularization as long as two rules are applied:

1. Data and program memories must be excluded when measuring the regularization of a single chip microcomputer.

2. The devices in all the chips must be included when measuring a multi-chip processor.

An indication of how regular past microprocessors have been is shown below:

$$8080 = \frac{4.6}{4.3} = 1.06 \qquad 8085 = \frac{6.2}{2.0} = 3.10 \qquad 8086 = \frac{29.0}{6.6} = 4.4$$

Analysis has shown that it should be possible to produce microprocessor designs with a regularization parameter between 10 and 20. If this can be achieved, it will reduce the layout effort in 1982 from 60 man years to 5 man years and allow us to utilize the technology to its fullest extent.

SUMMARY

The rapid evolution of microprocessor complexity, as well as the constant level of layout productivity, have caused manufacturers to reevaluate their VLSI design methodology. One part of this emerging methodology will be the use of regular structures in microprocessor design. In order to aid the designer in creating more geometric regularity into new chips, a measure of regularization has been proposed. This parameter would suggest that increasingly regular designs will not only solve the design complexity problem, but will also reduce the layout problem to a manageable level and thus allow microprocessor chips to fully exploit the new technology.

References:

1. Sutherland, I. and Mead, C., "Microelectronics and Computer Science", SCIENTIFIC AMERICAN, September, 1977