THE ROLE OF TEST CHIPS IN COORDINATING LOGIC AND CIRCUIT DESIGN AND LAYOUT AIDS FOR VLSI

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ABSTRACT

This paper emphasizes the need for multipurpose test chips and comprehensive procedures for use in supplying accurate input data to both logic and circuit simulators and chip layout aids. It is shown that the location of test structures within test chips is critical in obtaining representative data, because geometrical distortions introduced during the photomasking process can lead to significant intrachip parameter variations. In order to transfer test chip designs quickly, accurately, and economically, a commonly accepted portable chip layout notation and commonly accepted parametric tester language are needed. In order to measure test chips more accurately and more rapidly, parametric testers with improved architecture need to be developed in conjunction with innovative test structures with on-chip signal conditioning.

1. INTRODUCTION

The increasing complexity of VLSI circuits is forcing the development of coordinated aids for circuit design and layout, in particular aids that can be used to predict the performance of circuits prior to their fabrication. Key elements in the development of design and layout aids are microelectronic test chips, parametric testers, and data analysis procedures. Since test chips provide the input data for the logic and circuit simulators and the chip layout aids, it is essential that test chips be developed in concert with the simulators and layout aids.

Microelectronic test chips* have been used by the integrated circuit industry for many years. Typically, the test chips are substituted at several selected sites for integrated circuits on production wafers. The points in an integrated circuit production sequence where test chips can provide valuable information are illustrated in figure 1. This sequence shows the logic design sequence on the left and the circuit layout and fabrication

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*In the authors' view, the term test chip is preferred over the term test pattern which can be confused with a sequence of electrical pulses used to test a circuit. The preferred term used to describe this latter effect is test vector.

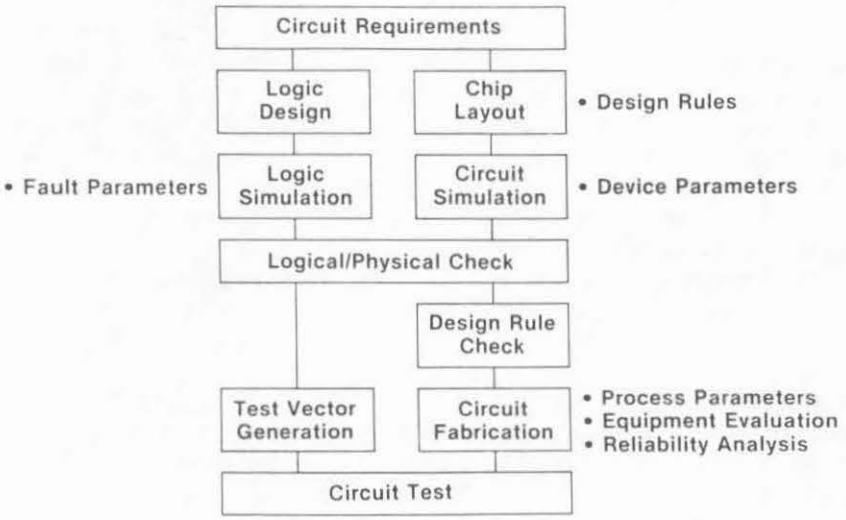


Figure 1. A simplified integrated circuit production sequence illustrating the points where test chips provide needed information.

sequence on the right. Before fabrication, cross checks are made to ensure that the physical design correctly implements the logical specification [1].

Traditionally, test chips have been used to supply process and device parameters and subcircuit data. In recent years, test chips have been used to evaluate such processing equipment as photomask aligners [2] and ion implanters. Also, reliability information has been obtained from test chips containing MOS capacitors which are analyzed for mobile oxide charge contamination and interface state densities [3]. In this paper we wish to highlight the role of the test chip as identified in figure 1 in circuit simulation, logic simulation, and chip layout.

2. CIRCUIT SIMULATION

The simulation of the dc and timing characteristics of a circuit is essential in identifying circuit design flaws prior to the fabrication of complex VLSI circuits. In this section, the circuit simulator requirements are discussed in terms of test structures for (a) acquiring device parametric data, (b) verifying the dynamic circuit performance capability of the fabrication process, (c) measuring intrachip parameter variations, and (d) evaluating the onset of small geometry effects.

Simulators such as SPICE [4] or MSINC [5] require device models, device parametric data usually collected from test chips, and geometrical layout information for the circuit being simulated. The device engineer "adjusts" various parameters in the simulator code so that the device models faithfully replicate the observed device performance. From discussions with industrial scientists, we found that the dc response and timing simulation of MOS digital logic circuits is judged as adequate for processes where both the design rules and fabrication procedures are stable. In such a stable environment, the devices can be modeled with the use of a mixture of empirical intuition and physical insight.

The predictive capability of circuit simulators is greatly reduced when the design rules change (e.g., devices become smaller) or when the process is changed significantly. For these circumstances more sophisticated device phenomena (e.g., short-channel effects) must be taken into account. In the long term, industry will need circuit simulation codes and data collection methodologies (based on test chips) that are easy to use and upgrade and can predict circuit performance as design rules and processes change.

A commonly accepted test circuit must be developed which can verify that the fabrication process is capable of producing circuits with correct dynamic (or timing) properties. Traditionally, ring counters which are characterized by their frequency of oscillation have been used for this purpose. However, the oscillation frequency can often not be adequately simulated (especially in MOS circuits) because many interdependent factors contribute to its magnitude. A candidate circuit should be easy to measure in chip form and its performance should be simple to evaluate.

As feature sizes become smaller, the ability to fabricate circuits with uniform features will become more difficult. As a result, the percentage

variation in device parameters will increase. This variation will make circuit simulation more difficult. It also poses a problem in the placement of test devices on a test chip, for a device located in one part of the chip can have significantly different characteristics from a supposedly identical device in another part of the chip. Such effects were observed by Ham [6] for the threshold of MOSFETs fabricated in silicon on sapphire. The variations can be either intrachip or interchip in nature.

To illustrate the importance of such parameter variations, we have measured the linewidth variations with the use of the cross-bridge test structure [7] shown in figure 2.* Using the test structure shown in figure 2, a single mask test chip was prepared on a 10X master reticle. The test chip was composed of an 12 by 20 array of identical test structures with a design linewidth of 6 μm. The final photomask was prepared from the master reticle by a step-and-repeat process. The photomask was used in conjunction with a contact printer and a photolithographic process to etch the test chip pattern into an 800-nm thick aluminum layer. The aluminum had been electron-gun evaporated and deposited on an oxide film thermally grown on a 2-in. (50.8-mm) diameter silicon wafer.

The linewidth variations shown in figure 3 are from a single row of test structures measured across the diameter of the wafer. The plot shown in figure 3 indicates that the linewidth varies periodically with the chip dimension of 250 mil (6.35 mm). This periodic or *intrachip* variation is superimposed on a nonperiodic or *interchip* linewidth variation due to those factors which affect the contact between the photomask and the photoresist-covered wafer. The periodic or intrachip linewidth variation is due to aberrations in the optics of the image repeater used to step and repeat the 10X reticle. Similar results have been reported for a 15-μm line [8].

The absolute magnitude of the variations shown in figure 3 is independent of the magnitude of the linewidth. Thus, the impact of such linewidth variations on device characteristics is quite dramatic especially for small devices. The linewidth variation for the lines shown in figure 3 is about 13 percent. For 1-μm lines, the variation would be 70 percent. These results illustrate the importance of the location within the test chip where "representative" device parameters are measured. Ultimately, the accuracy of the data entered into circuit simulators will be limited by both intrachip and interchip parameter variations.

The final item mentioned in this section concerns the development of test structures and evaluation techniques which tell when the models used in the circuit simulators are no longer valid due to the onset of small geometry effects. Of critical importance for future VLSI components are the

*The linewidth is determined after measuring the sheet resistance R_s which is determined from $R_s = (\pi/\ell n2)(\Delta V/I)$, where I is the current forced between I_1 and I_2 and ΔV is the voltage difference between V_1 and V_2. The linewidth W is given by $W = R_s L I^*/\Delta V^*$, where L is the distance between the voltage taps shown in the figure, I^* is the current forced between I_1^* and I_2^*, and ΔV^* is the voltage difference measured between V_1^* and V_2^*. A more detailed account of the measurement is given in reference [7].

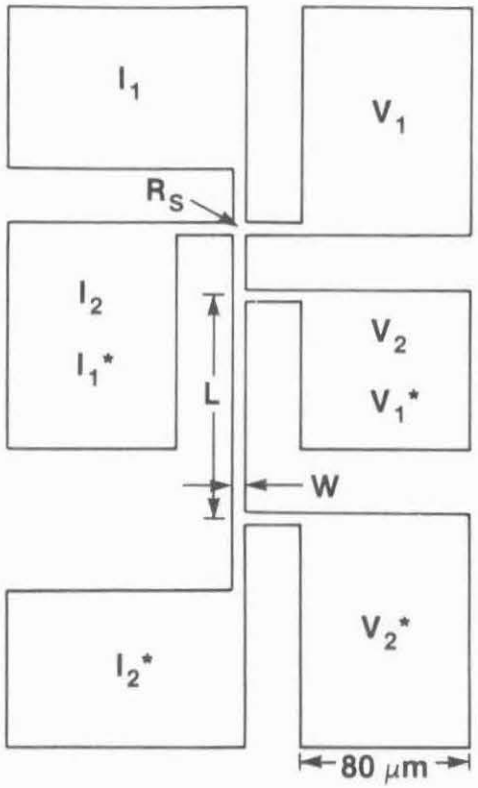


Figure 2. The cross-bridge test structure used to measure the sheet resistance and linewidth of a conducting layer.

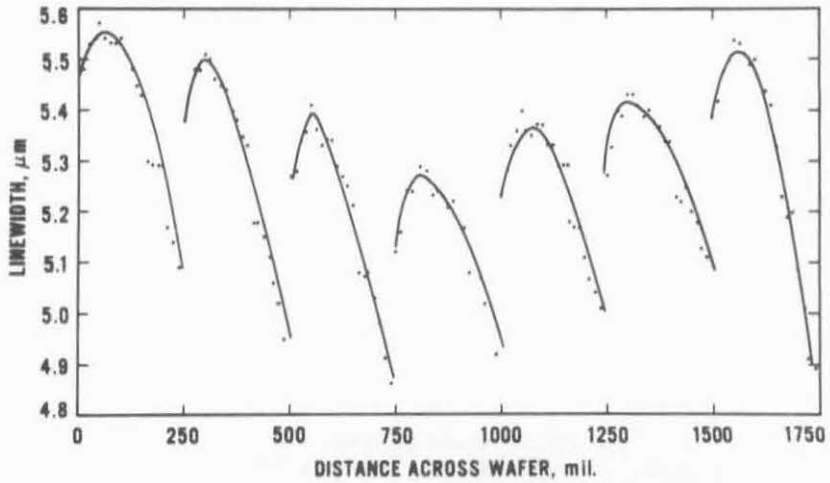


Figure 3. The variation of the linewidth as determined from an array of identical cross-bridge test structures as shown in figure 2. The period of the linewidth variation corresponds to the width of the test chip, 250 mil (6.35 mm). This periodic linewidth is due to aberrations in the optics of the image repeater used to step and repeat the 10X reticle.

evaluation of MOSFET short-channel effects and capacitor fringing field effects.

3. LOGIC SIMULATION

The logic simulation of the gate level performance of a circuit is essential in identifying logic design flaws prior to the fabrication of complex VLSI circuits. As shown in figure 1, the logic simulator can also be used to develop the test vectors used to test the circuit after fabrication. An accurate simulation depends on having proper fault models, correctly identified faults and their density, and detailed layout information.

An example of a test structure which can provide detailed information for fault simulation is shown in figure 4. This figure shows a MOSFET array which is composed of 100 devices where the gate is connected to the drain. This structure appears on test chip NBS-16 [9] which includes two p-channel and two n-channel MOSFET arrays. On a 3-in. (76.2-mm) diameter wafer, 380 arrays containing 38,000 MOSFETs were tested. The results shown in table 1 are from 26,760 MOSFETs located in the interior portion of the wafer. Both the fault location and the relative density of different fault types, both clustered and nonclustered, can be determined from the electrical data. A fault is considered to be clustered when two or more adjacent MOSFETs containing the same fault type are detected in an array. As seen in the table, the most frequent fault was #8, a combination of excessive leakage current and low breakdown voltage.

A major limitation of present logic simulators is their inability to properly model faults other than classical faults. The latter comprise those faults where signal lines are either shorted to the power supply (stuck-at-one), shorted to ground (stuck-at-zero), or simply open circuited. Sievers [10] has recently shown how the classical faults and open and short faults can be modeled for both nMOS and CMOS circuits. Any of the first five faults listed in table 1 could lead to a classical, open, or short fault. But the total of these five faults is only a small fraction of the total of the nonclassical faults, #6 through #13. Future logic simulators must have the ability to model such nonclassical faults in order to enable more realistic circuit fault simulations.

When using a logic simulator, it is essential that there be a one-to-one correspondence between the logic representation and the physical layout [11]. For example, the logic diagram shown in the upper part of figure 5 bears little resemblance to the accompanying circuit schematic. To illustrate, the wire D joining the two gates is not uniquely found in the circuit schematic. To perform a fault simulation where a classical fault (stuck-at-one or stuck-at-zero) is introduced on this wire is a meaningless exercise.

4. CHIP LAYOUT

Chip layout is a very important part of a VLSI design system because the layout influences all other parts of the system. For example, the layout data set can be used to derive the geometrical data needed by the circuit and logic simulators. In addition, the choice of layout notation can restrict

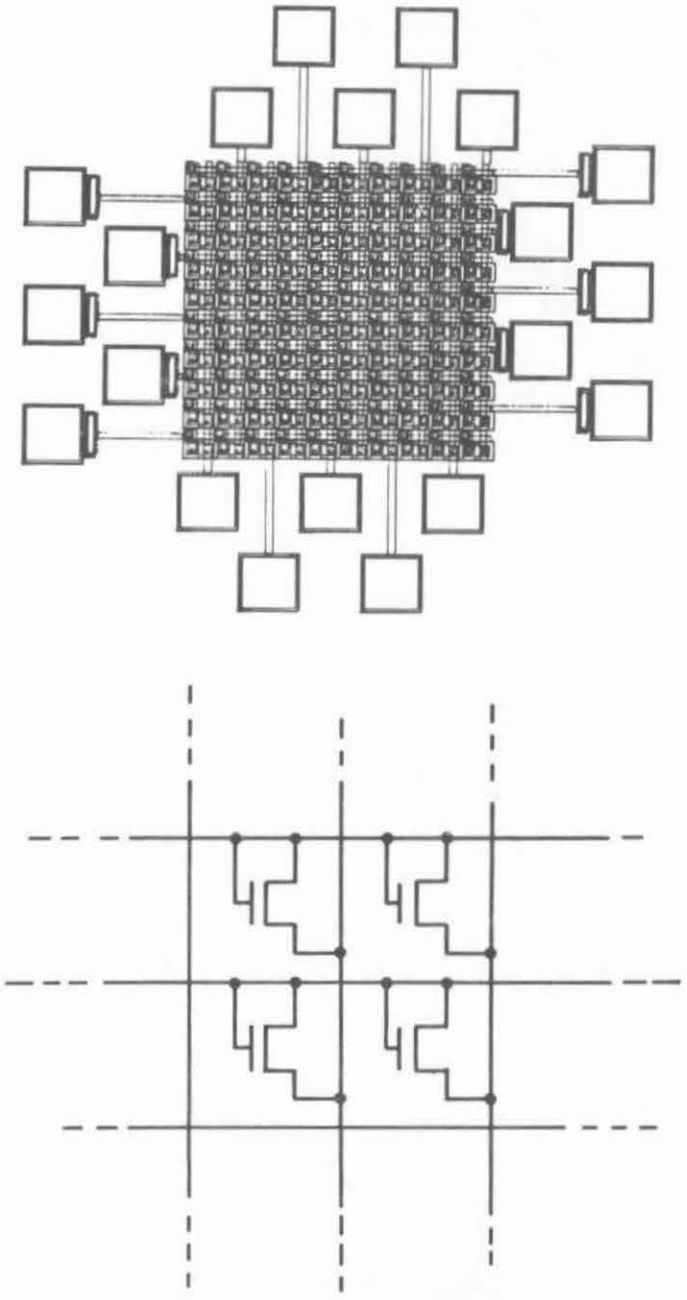
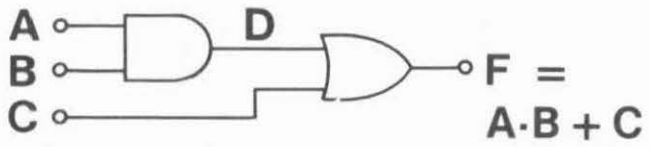


Figure 4. MOSFET array test structure consisting of 100 individually addressable transistors shown above. A schematic diagram is shown below.

Table 1. MOSFET Array Test Results.

Number	Fault	Number of Nonclustered Faults	Number of Clustered Faults
1	Poly void/break	4	0
2	Epi void	0	1
3	Metal void/break	0	0
4	Metal bridge	1	0
5	Gate short	4	0
	V_T I_L V_B		
6	- - L	5	0
7	- H -	25	0
8	- H L	62	0
9	L - -	1	1
10	L H -	0	1
11	L H L	0	1
12	H - -	2	2
13	H H L	0	1

V_T = threshold voltage; I_L = leakage current; V_B = breakdown voltage.
H = parameter too high; L = parameter too low.



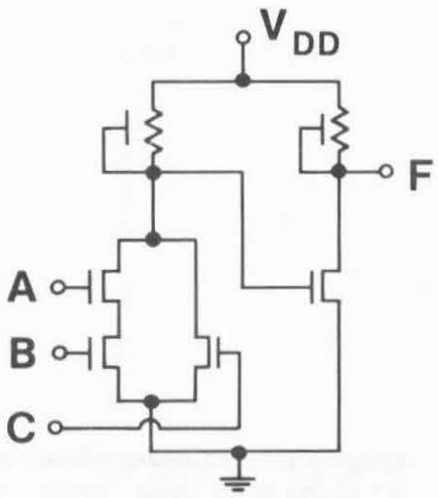


Figure 5. Lack of correspondence between the logic diagram and the circuit schematic in that wire D does not appear uniquely in the circuit diagram.

the portability of the design. In the authors' view, the chip layout methodology must allow for design portability so that circuits can be fabricated in facilities with different design rules. The idea is to supply different fabrication facilities with a chip layout description that can be adjusted to meet the design rules for that particular facility. This idea requires that the manufacturer adjust the chip layout pattern as it appears on the photomask to allow for changes in feature sizes during fabrication so that features appear with specific dimensions on the finished circuit. One layout representation that appears to be a candidate for such portability is symbolic notation [12].

An additional need in chip layout is to develop test structures that can be used to establish layout design rules. Structures useful for this purpose are known as random fault test structures where a feature (e.g., metal-to-silicon contact) is repeated many times within an array [13]. Arrays with different numbers of features are fabricated and tested for opens or shorts. The number of good features per fault characterizes the process. The test structures to be developed must be designed so that the intended fault is measured. Good design practice dictates that each probe pad used to contact an array accommodate two probes (Kelvin contacts) so that one can be assured that the probes are making contact [8]. In addition, the arrays must be designed so that interferences between other parts of the array are eliminated [14].

5. TEST CHIP

Despite the long history of test chip usage by the integrated circuit industry, there has been relatively little emphasis placed on the development of such chips. To make better use of test chips in the future, one must develop a coordinated metrological system including advanced parametric testers, commonly accepted parametric tester language, improved microelectronic test structures, and efficient information-handling procedures.

The first multifunction parametric tester specifically designed to measure test chips was commercially available in 1978 and now there are at least three systems which can be purchased [15]. The availability of these systems greatly enhances the use of test chips in production wafer-probe environments. The commercially available systems typically have a system architecture that is based on the mechanical switch matrix as seen in figure 6. The accuracy and precision of such systems is limited by noise introduced by the switch matrix and long leads. In addition, measurement times can be long when measuring low-level quantities. The authors feel that these limitations can be overcome by changing the system architecture to the pin-electronics approach [16] as seen in figure 6. Here the stimulus/measure (S/M) devices are physically located close to the wafer probes. In addition, the number of wafer probes can be profitably increased (20 to 40 in the example) because test structures addressed by a wafer-probe array can be measured simultaneously. Overall test times for the pin-electronics approach should be significantly reduced [17].

A commonly accepted parametric tester language is needed to facilitate the rapid, accurate, and economical transfer of test chip measurements. As is

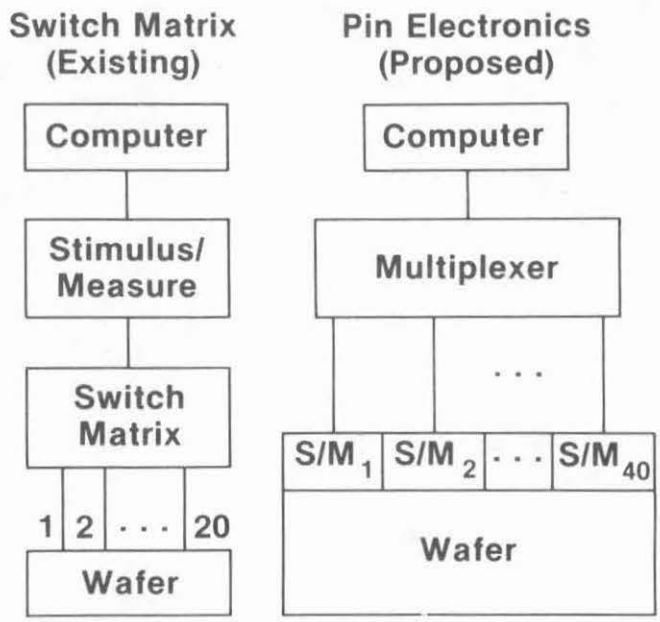


Figure 6. System architecture of multifunction parametric test equipment (existing and proposed [17]).

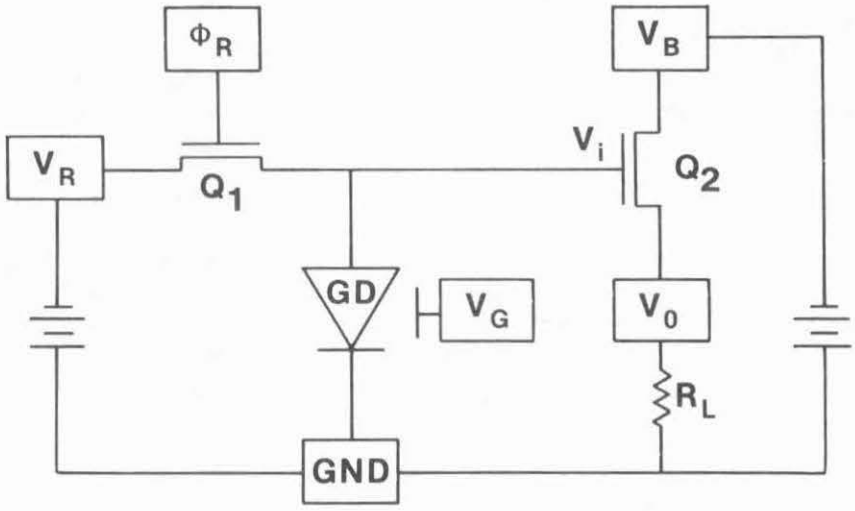


Figure 7. Schematic diagram of an integrated gated-diode electrometer. The boxes represent probe pads. The off-chip components are the two dc supplies and the resistor.

well known, software development costs are very expensive. There is an IEEE standard test language named ATLAS (Abbreviated Test Language for All Systems) [18] that was originally developed by the commercial airlines industry for testing avionics packages. Recently, a software package was developed which translates ATLAS into a test language used in the testing of digital printed circuit boards [19]. Currently, there is no comparable standard test language for parametric chip testers.

When developing new test structures, one must decide if there is a measurement advantage to be gained by incorporating a portion of the tester into the test structure. Such an advantage has been found with the integrated gated-diode electrometer shown schematically in figure 7. Low-level diode leakage currents can be determined by measuring the time decay of the output voltage V_o resulting from the momentary application of reverse bias voltage V_R to the gated diode GD through the MOSFET switch Q_1. The internal gated-diode current I is determined from the expression [20]:

$$I = (C/\beta)\ (-dV_o/dt)\ ,$$

where C is the diode capacitance and β is the incremental gain of MOSFET Q_2. The diode capacitance can be determined from $C = \varepsilon A/W$ where ε is the dielectric constant for silicon, A is the area of the diode, and W is the width of the depletion region. For a one-sided step junction, $W = [2\varepsilon(V_i + V_b)/(qN)]^{1/2}$ where V_i is the diode voltage, V_b is the built-in voltage, q is the electronic charge, and N is the dopant density. The dc gain of MOSFET Q_2 is determined from $\beta = \Delta V_o/\Delta V_i$ which is evaluated by closing the MOSFET switch Q_1 ($V_i = V_R$) and measuring V_o at two different values of V_R. The expression above assumes that the capacitance of the gated diode C is large compared to the gate-source capacitance of MOSFET Q_2. The test structure design shown in figure 8 obeys this restriction. The off-chip output resistor R_L shown in figure 7 is replaced by an on-chip load MOSFET Q_3 with its gate connected to the V_o point so that it operates in the saturated mode.

Another integrated test structure has recently been reported by Iwai and Kohyama [21]. This structure is shown schematically in figure 9. Here, the unknown capacitance

$$C_X = C_R\ [\beta(v_i/v_{oa}) - 1]\ ,$$

where C_R is a known reference capacitor, β is the ac gain of the output MOSFET, v_i is the rms value of the ac input signal, and v_{oa} is the output at v_o for v_i connected to point "a." To measure C_X, v_i is applied to point "a" and the MOSFET switch Q_1 is opened by properly biasing ϕ. The ac gain β is determined from $\beta = v_{ob}/v_i$ where v_{ob} is the output at v_o for v_i connected to point "b." In this measurement the MOSFET switch Q_1 is closed by properly biasing ϕ. This structure is useful in determining the value of the small capacitances typical of VLSI device geometries by connecting many capacitors into an array.

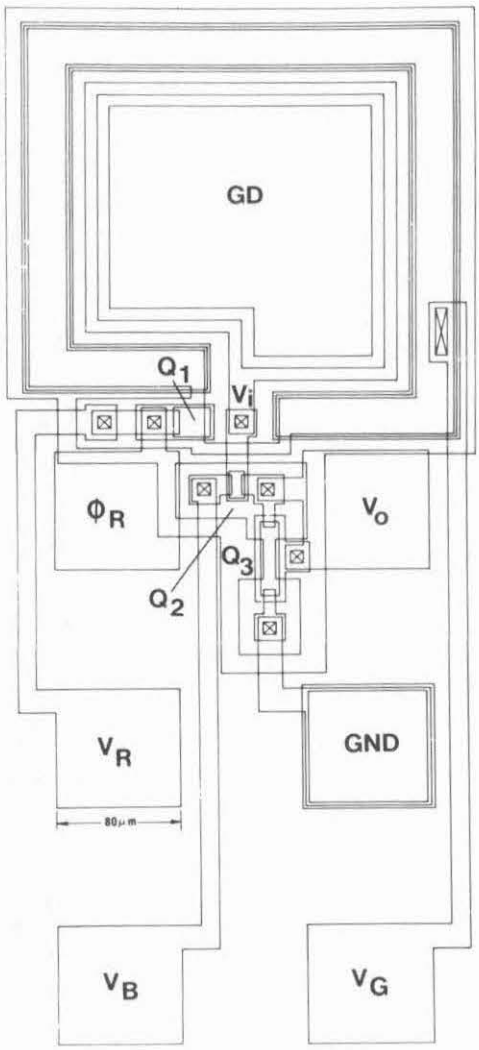


Figure 8. The integrated gated-diode electrometer test structure shown for a polysilicon-gate technology.

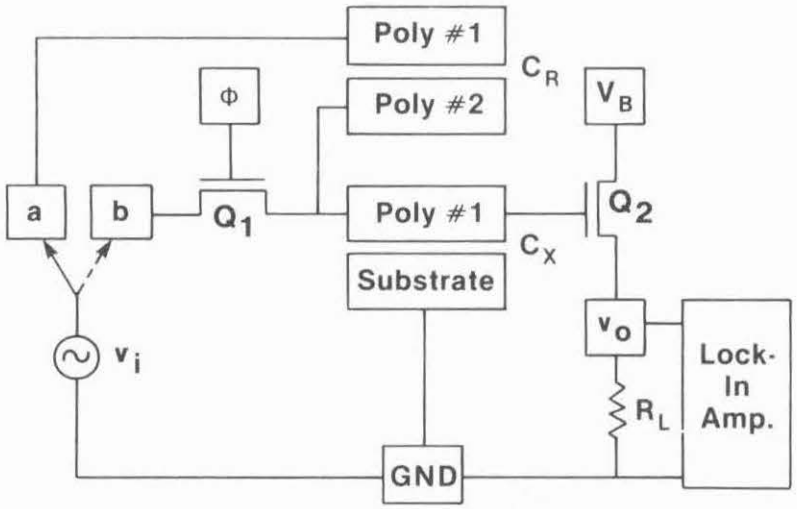


Figure 9. Schematic diagram of an integrated precision capacitance meter. The off-chip components are V_i, R_L, and the lock-in amplifier.

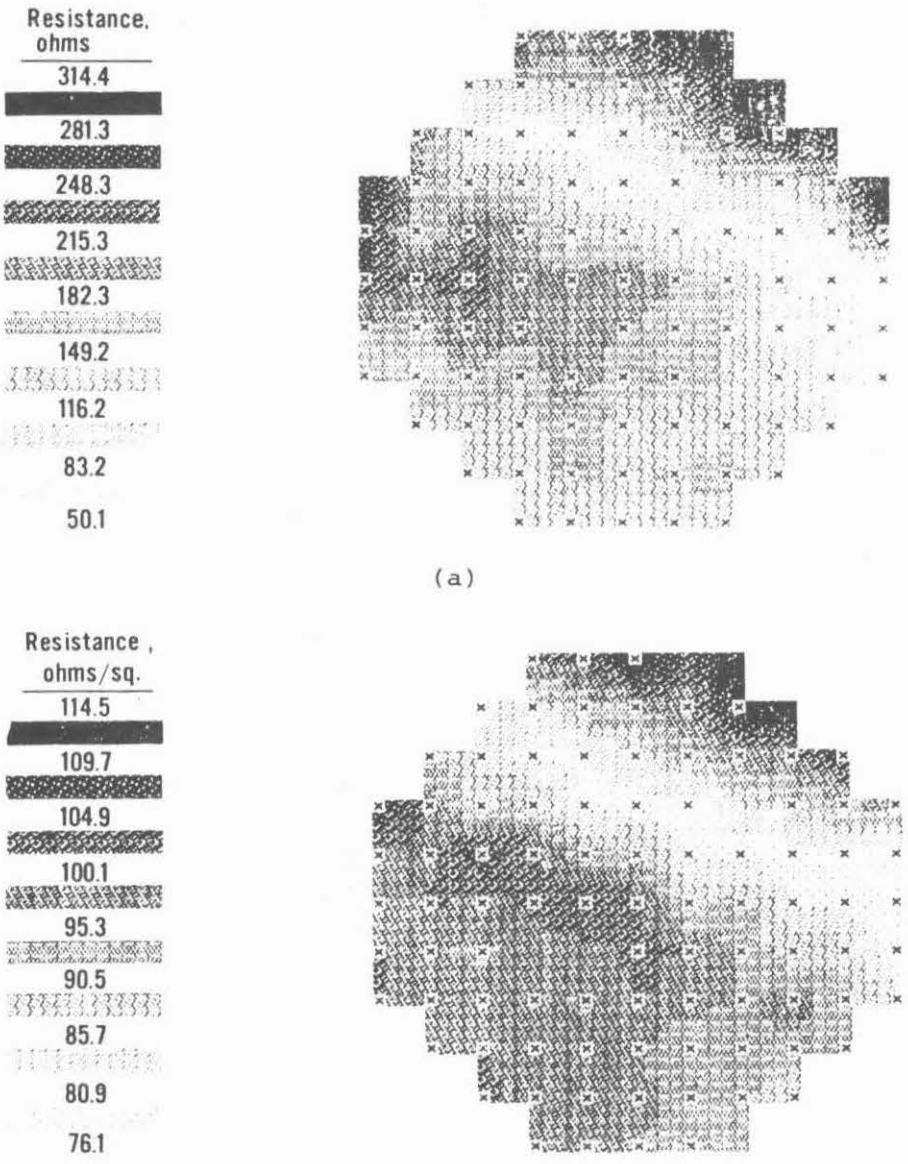


Figure 10. Wafer maps of the metal-to-n^+ contact resistance (a) and the n^+ sheet resistance (b). The high correlation between these two parameters leads to the conclusion that excessively high contact resistance was due to the lack of adequate control of a phosphorus implant process step.

Once the information has been collected from test chips, the data must be quickly analyzed to be of benefit. Wafer maps of a spectrum of parameters are crucial in identifying problems [22]. For example, a contact resistance problem was identified and correlated to variations in sheet resistance as shown in figure 10 [9]. The correlation was identified by observing a high correlation of these parameters from a host of other parameters [23]. The manufacturer of this wafer would not have identified this problem because his procedures called for only two test chips on each product wafer. Other information-handling techniques have been developed over the years [24]. The industry needs to fully utilize existing techniques and to search for more useful and efficient techniques.

6. CONCLUSION

Test chips have a role that goes beyond their traditional role involving process or subcircuit evaluation. The additional role involves supplying the data for the logic and circuit simulators and in setting the design rules for chip layout methods. The development of design aids and test chips must be coordinated to provide a well-integrated design system. In addition, new parametric testers are needed that can quickly supply data of increased accuracy. The development of such testers must be coordinated with test structure development so as to take advantage of on-chip signal processing. In addition, effective data-handling techniques (e.g., wafer mapping and data management) need further development so as to rapidly reduce data to a useful form. In order to transfer test chip designs quickly, accurately, and economically, a commonly accepted portable chip layout technique and a commonly accepted parametric tester language are needed.

7. ACKNOWLEDGMENTS

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