A SUBNANOSECOND LSI FAMILY FOR MAINFRAME TECHNOLOGY

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ABSTRACT

A subnanosecond LSI family is defined for next generation mainframes. It employs distributed on-chip regulation to reduce system power supply cost, stacked structures for delay-power improvement, on-chip test/diagnostic monitors and signature circuits to improve system maintainability.

CALTECH CONFERENCE ON VLSI, January 1979

SUMMARY

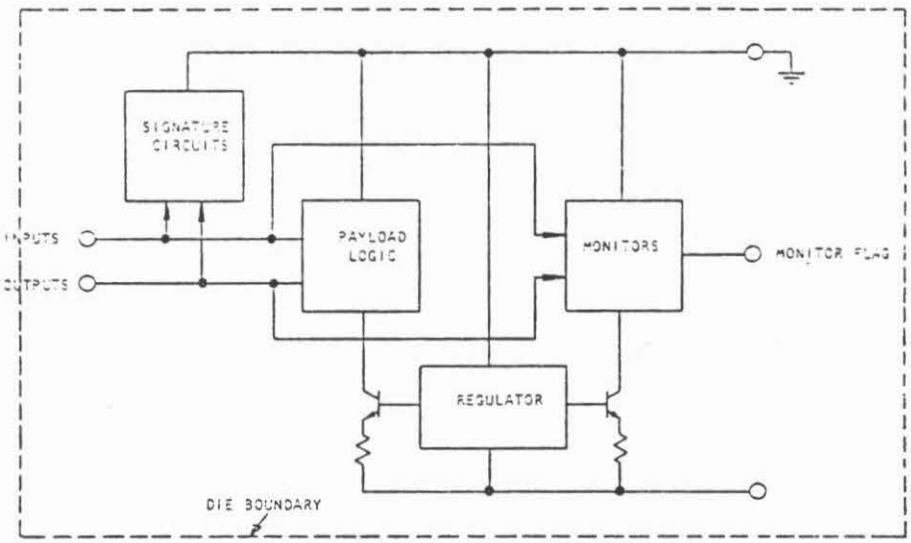
Progression of subnanosecond logic families into large scale integration has opened up new directions and alternatives for high speed mainframe design. The diversity of hardware considerations, however, necessitates an in-depth study to outline optimal configurations for next generation high speed LSI machines. Approaching cost, performance, reliability and maintainability from top down, a 4.65 V+ 18% subnanosecond current switching LSI family has been defined. This LSI circuit family employs an innovative, efficient, low overhead local regulating scheme (Figure 1). It has an efficiency of 97%, occupies an area of less than 200 x 200 for 400ma drive capability. For regulator performance characteristics see Figure 2. Due to the much relaxed power supply tolerance, a 3-phase unregulated power system may be used in conjunction with tolerant distribution, thus resulting in significant cost reduction (Figure 3).

Due considerations have been given to the selection of the supply voltage range so it can accommodate a diversity of circuit types such as RAM and PROM combined with logic elements on one chip. Figure 4 depicts the minimum voltage required for high speed memory and logic. As memory circuits require extra voltage over single level logic gates, an innovative power saver bus (Figure 5) improves the delay-power product of the LSI family. A stacked gate structure fully utilizes the supply voltage for output gates and internal non-series-gated gates.

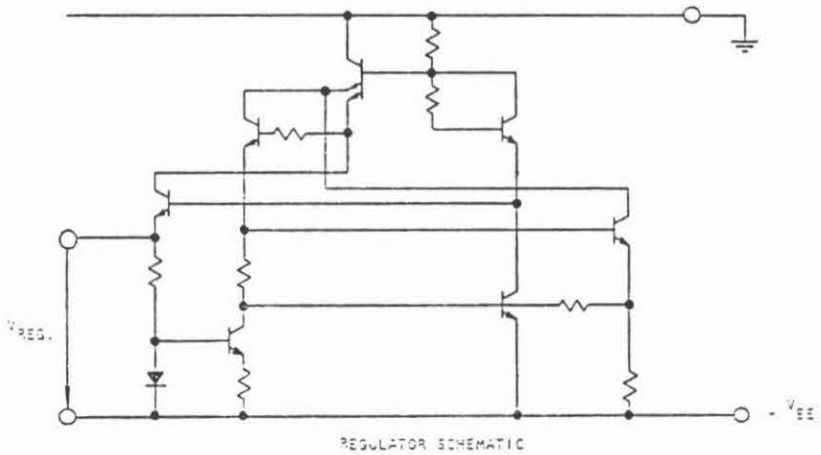
Having defined voltage supply and distribution, and the thermal system conditions , a set of RAM, PROM, payload logic, and monitor circuit cells designed within these boundaries will be described.

All inputs are buffered by emitter followers to reduce AC and DC loading while output structures are designed to serve as source terminations. Discrete active or passive components are neither required nor allowed and the packaging of the LSI system becomes truly homogeneous and reliable. Maintainability is enhanced by implementing on-chip test and diagnostic monitors together with fault isolation facilities. The monitors (Figure 6) assist in factory and field testing and in troubleshooting of the interconnecting signal and power nets with the possibility of an anticipatory maintenance concept. Chip-engraved signatures simplify pseudo random testing of LSI devices even while in-situ. The on-chip signature circuits and their interaction with a hand-held pseudorandom tester will be described.

This LSI philosophy will stimulate advances in mainframe design which demand new concepts in architecture and system partitioning beyond simple cost/performance tradeoffs.



BLOCK DIAGRAM OF LSI DIE CONTENT



REGULATOR SCHEMATIC

FIGURE 1

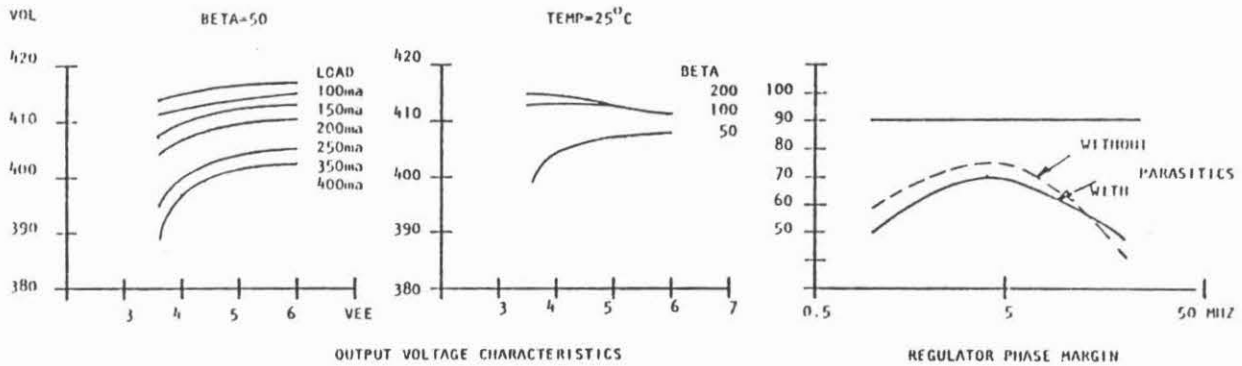

VOL
BETA=50
420
410
400
390
380
LOAD
100ma
150ma
200ma
250ma
350ma
400ma
3
4
5
6
VEE
TEMP=25°C
BETA
200
100
50
7
OUTPUT VOLTAGE CHARACTERISTICS
100
90
80
70
60
50
WITHOUT
PARASITICS
WITH
0.5
5
50 MHZ
REGULATOR PHASE MARGIN

FIGURE 2

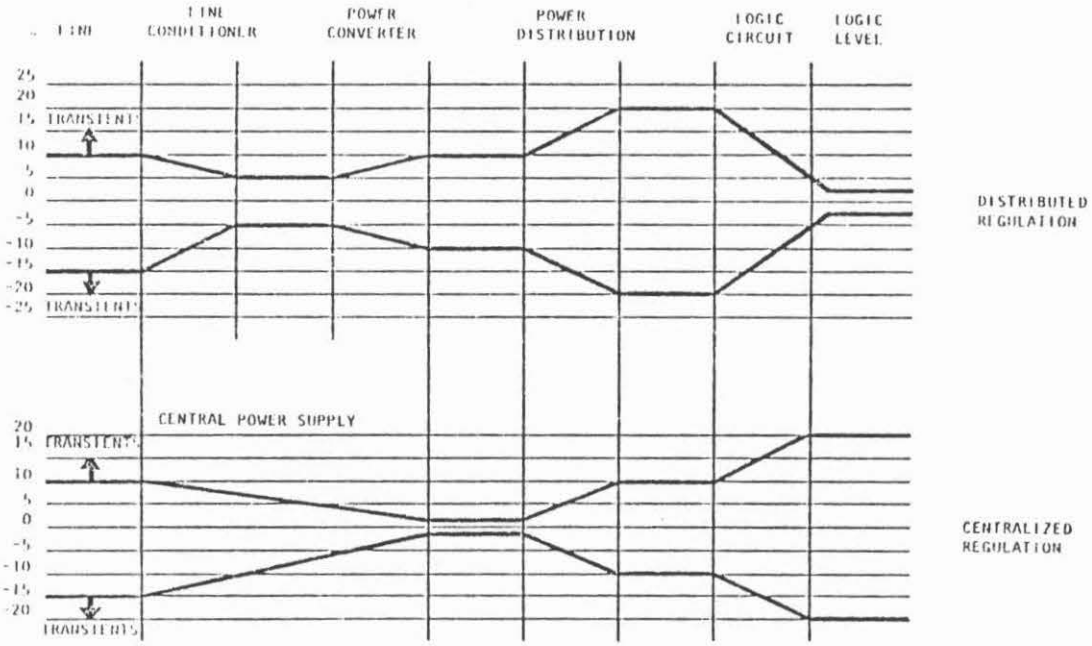

LINE
LINE CONDITIONER
POWER CONVERTER
POWER DISTRIBUTION
LOGIC CIRCUIT
LOGIC LEVEL
25
20
15
10
5
0
-5
-10
-15
-20
-25
TRANSIENTS
TRANSIENTS
DISTRIBUTED REGULATION
CENTRAL POWER SUPPLY
20
15
10
5
0
-5
-10
-15
-20
TRANSIENTS
TRANSIENTS
CENTRALIZED REGULATION

FIGURE 3

CIRCUIT TYPE	MINIMUM VOLTAGE REQUIRED	COMMENT
PROM	3.8	FUSIBLE LINK
LOGIC	3.4 / 3.8	3-4 LEVEL SERIES GATING, E.G., 1/4 AND 1/8 MUX
RAM	3.8	EMITTER COUPLED MEMORY
ROM	1.9/2.8	HIGH/LOW POWER DESIGN

ASSUMPTION:

1.2V VOLTAGE REFERENCE

400MV MAX. FORWARD BIAS ACROSS BASE COLLECTOR JUNCTION.

FIGURE 4 MINIMUM SUPPLY VOLTAGE FOR CURRENT MODE SWITCHING CIRCUITS

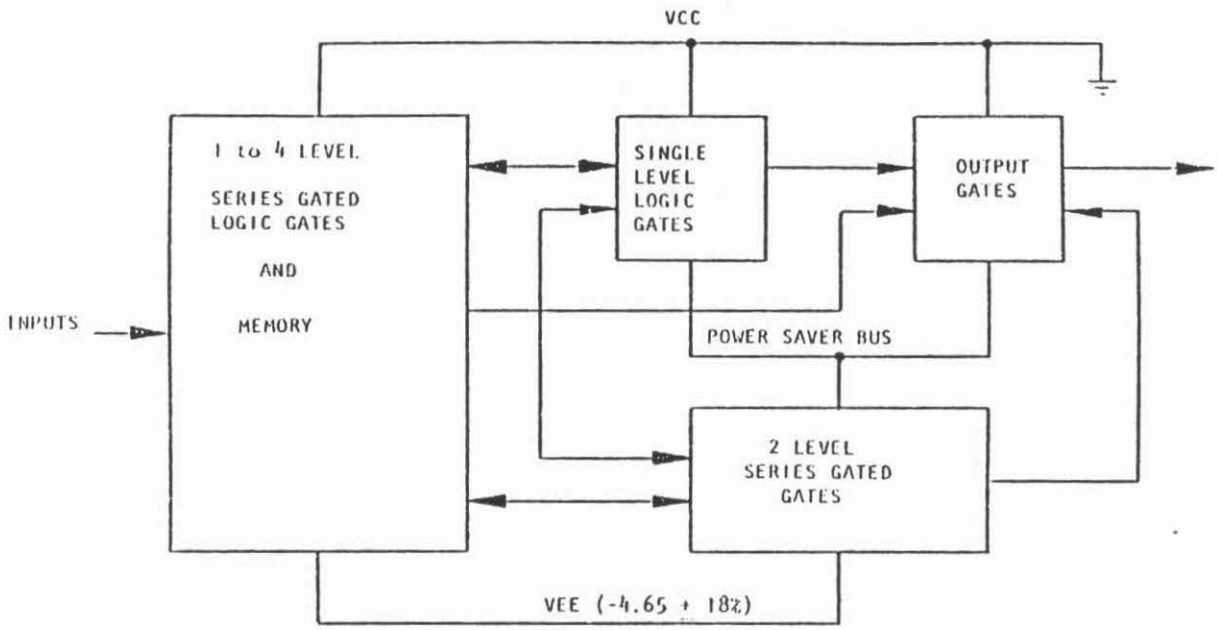
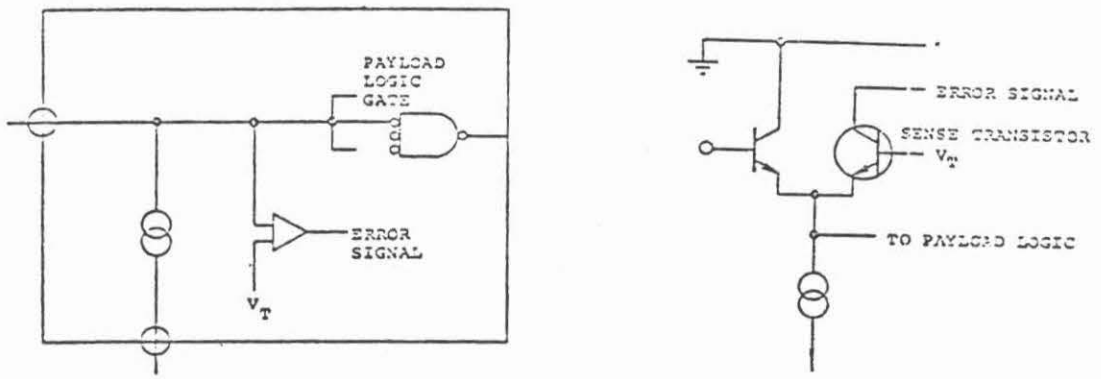
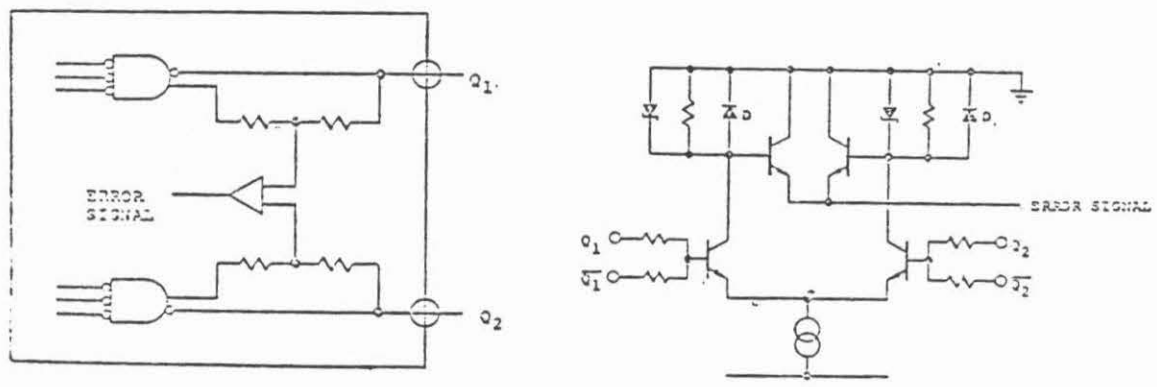


FIGURE 5 SUBNANOSECOND LSI CHIP CONFIGURATION



INPUT MONITOR



OUTPUT MONITOR

FIGURE 6