A SIMPLE TWO-LAYER ALUMINUM METAL PROCESS FOR VLSI

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I. Introduction

The use of two levels of metal interconnect lines in an integrated circuit chip layout is a very desirable feature that allows higher density and greater freedom in the placement of the active components. In spite of these benefits it has often been avoided in the design of integrated circuits. For many applications the cost of the extra processing steps is not justified. In the case of MOS technology, long diffusion runs can be successfully used. In silicon gate MOS the polycrystalline silicon itself provides, with some restrictions, a second level of signal interconnect lines. However other technologies, for example I^2L, need a second layer of low-resistance metal interconnect to effectively utilize the chip area. While conceptually simple, two-layer metal processes have proved to be quite difficult to implement. This paper describes a relatively simple two-layer metal process that is well suited to university laboratories and others with limited facilities.

II. Current Practice

The principal problem encountered with two-layer metal processes is due to the surface topography of the insulating layer at the edges of the first layer of metal. The straightforward process for two-layer metal would be as follows. The first layer of metal is deposited and delineated by photoetching in the normal manner. A layer of insulator, most probably silicon dioxide, is then added by chemical vapor

deposition (CVD) on top of first layer metal. Holes are opened through the oxide by photoetching to allow contacts between the two layers. The second layer of metal is then deposited and delineated.

Two problems encountered with this simple procedure make it unworkable. One problem is that the low temperature CVD oxide used with aluminum processes etches very rapidly, making conventional wet etching processes hard to control. The oxide cannot be "densified" at high temperature because of the properties of the silicon-aluminum system. The second and much more severe problem stems from the surface topography of the CVD oxide layer at the edges of the first layer metal. The vapor deposition process, particularly when done at atmospheric pressure, increases the steepness of steps on the surface as shown in Fig. 1. Low angle scanning electron microscope (SEM) examinations of actual structures verify this. Figure 2 is the edge of an aluminum run covered with 5000 Å of CVD silicon dioxide deposited at atmospheric pressure. Addition of phosphorus to the oxide does not help. If anything it makes the edge profile steeper. When second layer metal is deposited on this vertical step, coverage is not good and it often does not survive the etching process as shown in Fig. 3.

Numerous approaches have been taken to solving this problem. Careful control is maintained over the relative thickness of the three layers involved. The CVD oxide and second layer metal will each be about twice as thick as the first layer metal. Such thick layers result in large feature size and create internal stress cracking problems.

A more fundamental approach is taken in those processes that "taper" the edge of the first layer metal. A gentle slope at the edge of first layer metal will be maintained by the CVD oxide. This prevents breaks in the second layer metal. Taper etch processes in general depend on "controlled undercutting" of the photoresist caused by a thin, rapidly-etching layer between it and the metal. One such

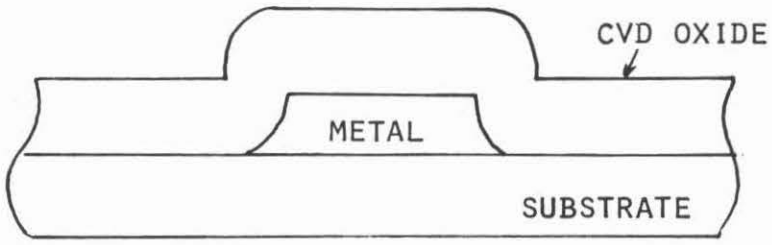

Fig. 1. Cross section of first layer metal covered with CVD oxide.

Fig. 2. SEM photo of edge profile of CVD oxide-covered metal.

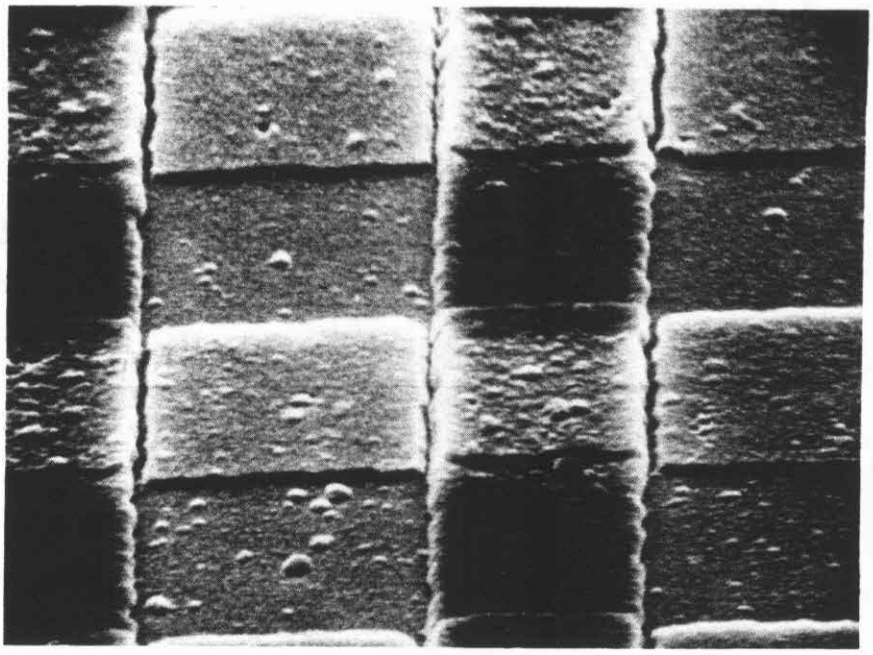

Fig. 3. Metal breaks in second layer metal at edges of first layer metal.

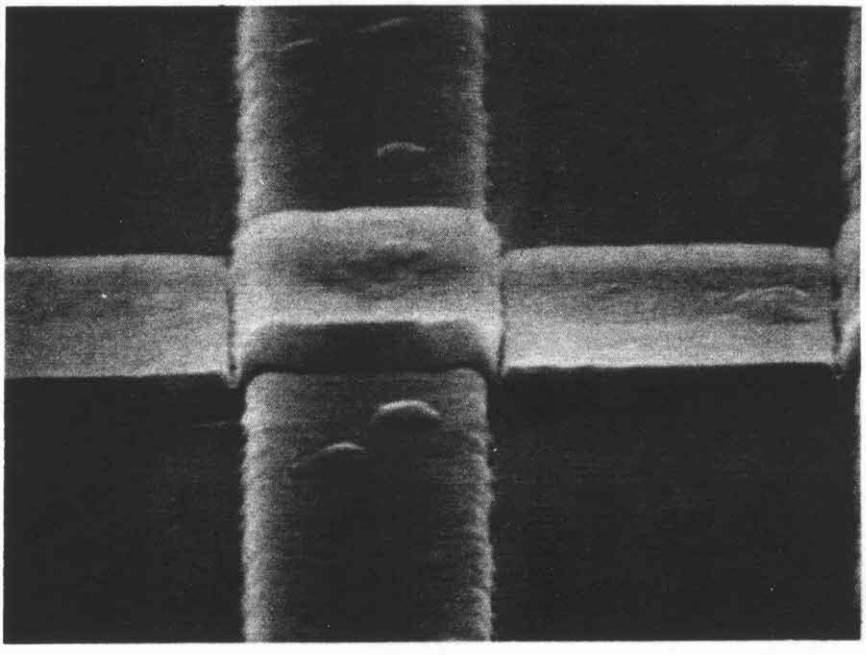

Fig. 4. Inferior metal coverage over sharp edge profile.

process is described by Wilson and Ghate [1].

Other methods improve the metal coverage over the steps by elaborate deposition apparatus. In one commonly used method the metal is sputtered onto high-temperature substrates in a rotating system. Because of the high temperature, the metal atoms have significant mobility once they are on the surface. Obviously this requires expensive equipment.

A direct and successful approach when conditions permit its use is a change in the physical nature of either the interlayer insulator or the process by which it is deposited. If the insulator can be deposited as a liquid, or liquefied after deposition, the surface energy will smooth out the surface. Such an approach is used in the usual silicon gate MOS process. The insulator layer (SiO_2) on top of the patterned polycrystalline silicon is formed by CVD. As deposited it shows the same edge profile problems that are being discussed here. However, it is often deposited in two layers. The top layer contains several percent P_2O_5, which lowers the softening temperature enough that, following deposition, it can be heated and allowed to flow. The flow eliminates the sharpest surface features and makes possible good metal coverage. Unfortunately this procedure requires temperatures too high to be used with two-layer aluminum.

In the process reported here, the interlayer insulator is an organic polymer which is deposited as a liquid using a conventional photoresist spinner. It cures to a polyimide which can withstand the temperatures [2] encountered in the wafer processing that follows second layer metal and in the die-attach, wire-bond, and package-sealing operations.

III. Polyimide Film as Interlevel Insulator

Several researchers have reported on the use of polyimide in planar structures. Among them are Sato, et al. [3] who describe a

multilayer metal interconnection technology in which holes for the interlayer electrical contacts are opened by a uniform removal of the polyimide down to "bumps" in the first layer metal. More recently Yen [4] described a low-cost polyimide interlayer insulation process. A polyimide passivation reliability study was reported by Gregoritsch at the 1976 Reliability Physics Meeting [5], and it has been reported that IBM Corporation is using a polyimide interlevel insulation in a new 65 K RAM chip [6].

IV. Polyimide Photoresist Two-Layer Metal Process

This process uses a photoresist* [7] as an interlayer insulator which contains sensitizers and precursors to polyimide. Following exposure and development, proper curing steps convert it to a polyimide which is thermally stable above 400°C. Because the interlayer insulator is deposited as a liquid, it gives a surface profile that is smoother than exists under it. As it is also a photoresist, no additional layers must be used to photoetch via holes. The process as developed in these experiments follows:

1. Finish wafers through first layer aluminum metal using the standard process. The metal must be given an alloy at as high a temperature as any of the subsequent processing.
2. Deposit by CVD methods about 1000 Å of SiO_2. Use of this oxide was found to give better adherence of the polyimide than did the aluminum alone.
3. Treat the surface with a coupling agent to promote adherence of the polyimide-based photoresist. We used hexamethyldisilizane (HMDS) diluted in Freon TF (1-1-2 trichlorotrifluoroethane) in the ratio of two parts HMDS to one part Freon TF, applied to the wafer on a conventional photoresist spinner at 2500 rpm.

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* These experiments used PR-514, a product of GAF Corporation. Since this work was done, that organization sold its photoresist business. It is not known at this time if this particular photoresist will continue to be available.

4. Immediately coat the wafer with the photoresist on the same spinner at 2000 rpm. This speed gives a layer approximately 1.4 μm thick.
5. Bake in nitrogen one hour at 80°C.
6. Align mask and expose. The resist is not very sensitive and about one minute UV exposure is required. Resist is positive working.
7. Develop 20 seconds in the developer supplied by the manufacturer. Rinse in deionized water and air dry for 15 minutes.
8. Reexpose the remaining photoresist without a mask to decompose any remaining sensitizer. Exposure should be at least twice the preceding exposure.
9. Bake the wafer in a series of steps beginning at 140°C for 15 minutes, and increasing the temperature about in 50°C increments, finishing at 440°C in N_2 for 5 minutes. The lower temperature bakes were done on a hot plate while the 440°C temperature bake was in a standard diffusion furnace.
10. Etch the 1000 Å of CVD SiO_2, which is now exposed under the open via holes, in standard buffered HF-based etch. Do not overetch.
11. Deposit second layer metal and finish the wafers normally.

After the polyimide has been exposed to 440°C it is not appreciably attacked by the usual photoresist strippers so it needs no protection during the photosteps which delineate second layer metal.

V. Results

This procedure was evaluated using a test pattern containing many metal crossovers and on an integrated circuit built with two-layer metal.

A comparison of the quality of metal crossovers obtained with polyimide and with CVD SiO_2 is shown in Figs. 4 and 5. Figure 4 shows a crossover obtained with the low temperature CVD SiO_2 and electron beam evaporated aluminum. Figure 5 shows a crossover fabricated from

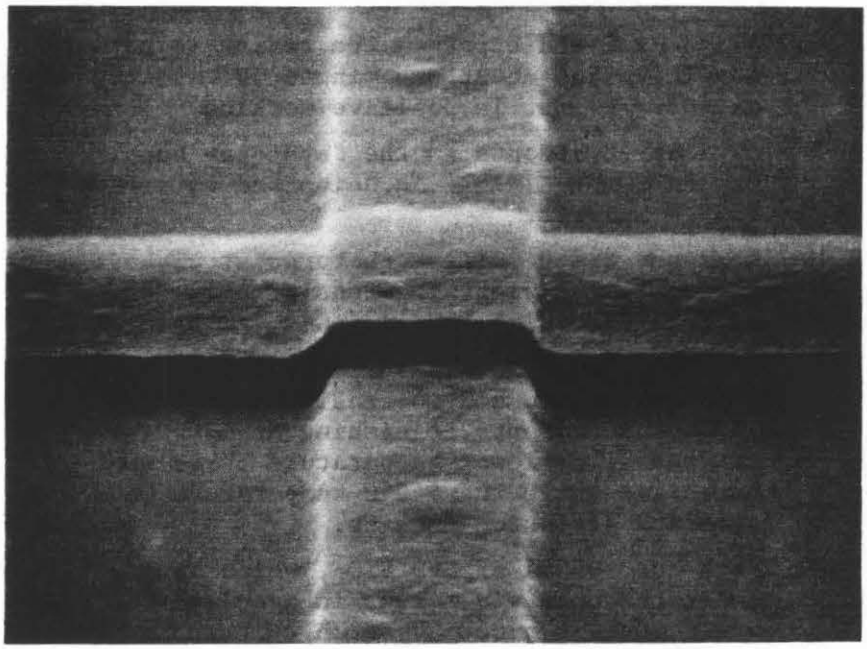

Fig. 5. Improved metal coverage over polyimide-covered first layer metal.

the same set of masks using the photoresist procedure described here. Note the much improved coverage where second layer metal crosses first layer metal. The advantage of the polyimide-covered surface is the more gentle slope at the edges of first layer metal.

A two-layer metal pattern containing 600 crossovers was built to check the incidence of metal breaks over the steps, the interlevel resistance and the ability of the polyimide to withstand thermal stress. The total area in which the two layers of aluminum are separated by polyimide was 6×10^{-4} cm^2. The incidence of metal breaks was extremely low. Too few breaks were found in these experiments to allow statistically meaningful yield predictions.

The structure was subjected to temperature cycling between +150°C and -40°C. First the pattern was heated to 150°C in air for one week with a constant 10 volts applied between the layers. Resistance between the layers was steady at 2×10^{11} Ω at 150°C. Then the structure was cycled between -40°C and +150°C six times with the interlayer resistance measured at each temperature extreme with 10 volts applied. At -40°C interlevel resistance was 2.5×10^{13} Ω and at +150°C interlevel resistance was 2.3×10^{11} Ω. Heating and cooling rates were about 40 degrees/minute. At the end of the tests, all metal runs were still continuous and no interlevel shorts observed.

A simple 1024-bit I^2L read-only-memory, organized as a 16 x 64 array, was built using this two-layer metal process to verify the ability of this process to actually produce an LSI circuit. A functionally good chip was placed on high temperature life test at 100°C and normal operating voltages and signals applied. Operation continued uninterrupted for over 6000 hours with no apparent degradation.

VI. Discussion and Conclusions

A two-layer metal process suitable for experimental two-layer aluminum metal has been described. It requires no additional equipment

over that required for the simplest single-layer aluminum and CVD SiO_2 processes. The interlevel insulator is a dual layer consisting of 1000 Å of CVD SiO_2 and about 1 μm of polyimide. The polyimide is obtained from a positive working polyimide-based photoresist. Interlayer contact holes are formed by exposure and development of the layer when still in the photoresist form, thereby eliminating many process steps used for polyimide layers that are deposited in the pure form. The polyimide shows no degradation when exposed to temperatures of 440°C in nitrogen and therefore circuits incorporating this layer will withstand normal packaging operations.

Acknowledgment

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