

ABSTRACT

Timing Considerations in Logic Arrays and Their Importance
to Self Timed Digital Circuits

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Abstract: This paper presents a method for the design of self timed circuits on an integrated circuit that takes advantage of certain temporal constraints that are realizable in logic arrays.

This method of design recognizes two distinct environments for circuits, the local environment and the global environment and further recognizes that the assumptions regarding the temporal characteristics of the system that may be valid in the local environment may not be valid in the global environment.

This paper shows how self timed circuits can be systematically designed on a single chip using assumptions reasonable for components on a single chip.

This paper is based on our work on Structured Logic Arrays (SLAs) and first explains the intricacies of the temporal constraints implemented in the structured array and then shows how one can take advantage of these constraints in the design of self timed circuits. In this structure, for example, it is possible to design an asynchronous sequential state machine with non adjacent transistions without getting into hazardous conditions. What is presented is related to Petri nets and their realization in circuits.

The circuits that are designed using this method are very regular in structure and are efficient in utilization of chip area. Furthermore, fairly large integrated circuits can be designed relatively fast using this method. Examples of some chip designs are presented.