ELECTRON BEAM TESTING AND RESTRUCTURING OF INTEGRATED CIRCUITS*

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Dramatic improvements in the cost, performance, and reliability of a digital system can be obtained if the system is integrated on a single chip. Many systems are sufficiently complex that the die size resulting from integration would be very large with a low probability of producing a perfect, functioning die. Since there is a real need for larger integrated systems than can be fabricated free of defects, it is likely that techniques which can locate and "wire-around" defects will be useful and will allow the die-size to increase, perhaps to full-wafer size.

A plausible scheme for fabricating a large system is:

(i) Design the large-scale system in a highly modular fashion. Partitioning into subsystems should stress minimum interconnection requirements between the subsystems, complete testability of each subsystem, and minimum number of subsystem types. This last requirement suggests that one should try to design and fabricate a single subsystem type, and that each subsystem would be assigned unique functions by a customizing operation. Finite state machines containing PLAs or ROMs are examples of subsystems which could be easily customized.

(ii) Customize and test the individual subsystems. If a particular subsystem does not function properly, a spare one would be customized and tested.

(iii) Interconnect working subsystems to form the large-scale system.

To construct such a system a flexible tool is required to allow subsystem customization, testing, and interconnection. The objective of this paper is to demonstrate that a scanned electron-beam provides this flexible tool. Specifically, the electron beam can be used for three essential functions:

(1) Input injection: the electron beam can be used to apply inputs and to alter the logical state of a subsystem under test.

(2) Output sensing: the electron beam can be used to sense the presence of a "zero" or "one" state at any one of a large number of test points.

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(3) Non-volatile restructuring: the electron beam can be used to open or close switches in the subsystems in a non-volatile manner. The opening and closing of switches is used to provide customization within the individual subsystems as well as control of the discretionary interconnect between working subsystems.

A variety of physical effects including charging and discharging of surfaces[1], voltage contrast[2], electron-beam induced current (EBIC)[3], melting or vaporization[4], eutectic-formation[5], threshold shifts in MOSFETs[6], and decomposition of organometallic vapors[7] may occur when an electron beam interacts with matter, and these effects could be exploited in an electron-beam testing and restructuring tool. Earlier work on electron beam testing of integrated circuits has centered on voltage contrast examination of chips for failure analysis, or stroboscopic measurement of waveforms. Generally a raster scan of the electron-beam is generated and an image of the chip is displayed or, alternatively, a single point is probed and a waveform is viewed on a CRT. The emphasis of the work presented here is to develop methods for computer-controlled electron beam testing of wafer-scale circuits, including restructuring techniques. This emphasis has the following implications:

(1) Input injection, output sensing, and programming of non-volatile switches must all be achievable in a single system.

(2) The test point to be probed or switching element to be programmed is selected by a computer-controlled deflection of the beam to the appropriate coordinate. The beam is unblanked only over selected points, so the entire circuit is not exposed to the beam.

(3) Testing can be fully automatic since a mask level description provides coordinate information for the electron-beam system. Potentially, node extraction and switch level simulation[8] can be used to generate test sequences automatically from the mask description.

(4) The objective is to perform only functional testing (i.e., checking for logical ones or zeroes), not parametric measurements.

(5) The integrated circuits must be designed to be compatible with electron beam testing. Specific structures incorporated in the mask-level specification make the electron-beam testing and restructuring possible. A wafer-scale power grid is used to supply power during electron beam testing.

Figure 1 illustrates a possible layout for a wafer-scale electron-beam testable system. The central portion of the wafer containing active subsystems and discretionary interconnect would be probed only by the electron beam. Some large test and power pads at the wafer perimeter could be contacted by relatively large probes in the cassette which holds the wafer in

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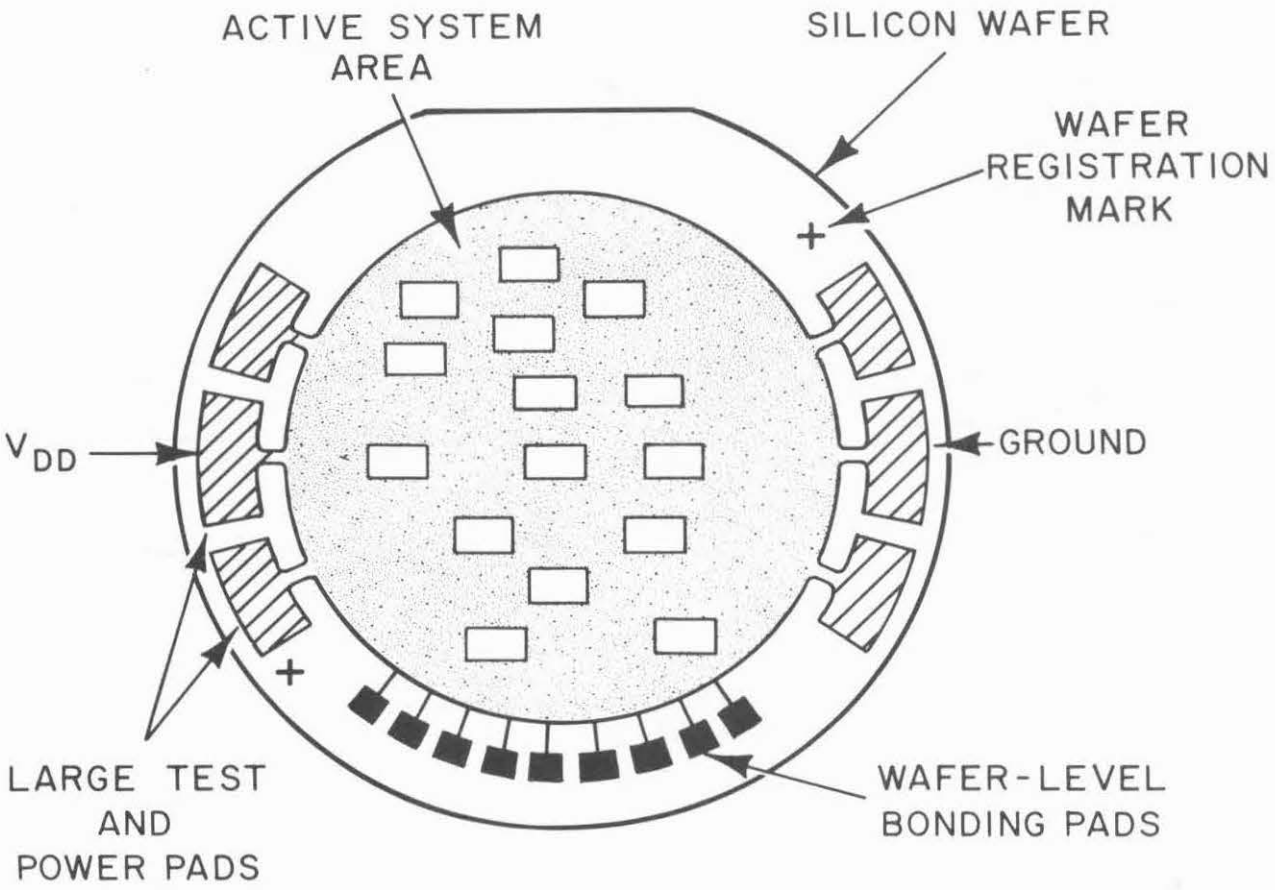


FIGURE 1: A possible layout for a wafer-scale system designed for electron beam testing and restructuring.

electron beam system. Only a very limited number of these pads would be required since the electron beam multiplexes use of the pads. A set of wafer-level bonding pads would be used to connect the wafer-scale system inputs and outputs in the final package. Figure 2 illustrates schematically a possible arrangement within the active subsystem area.

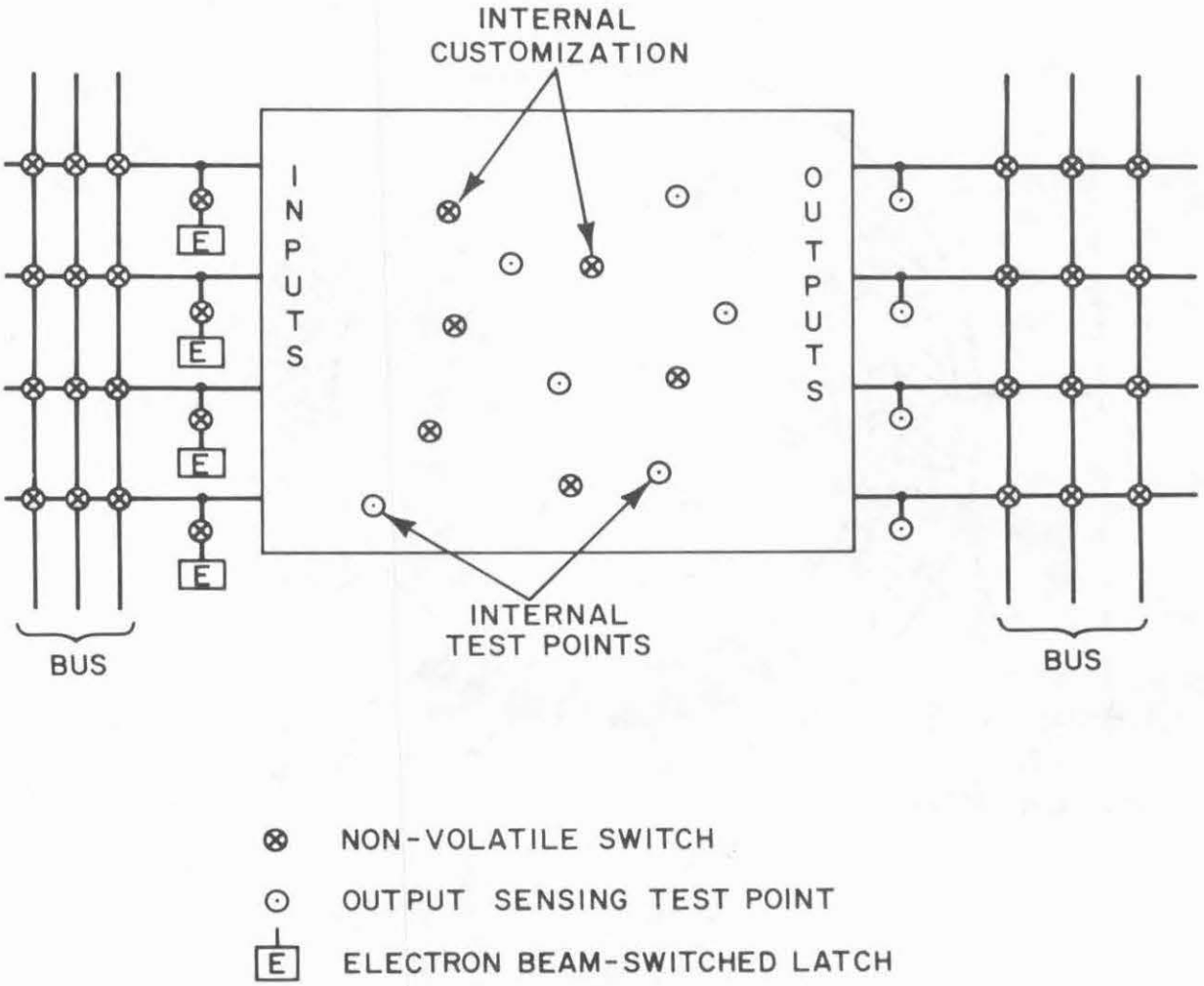


FIGURE 2: A schematic representation of a subsystem designed for electron beam testing and restructuring. ESLs can be used to apply inputs to the subsystem and sensing points are provided within and at the outputs of the subsystem. Non-volatile switches provide subsystem customization as well as flexible interconnect.

LOGICAL "OUTPUT" SENSING TECHNIQUES

Only specific techniques which are useable with n-channel MOS (NMOS) technology and which require no significant modification of our commercially available ETEC LEBES-D electron beam lithography system will be described. Since the system is also routinely used for mask-making and direct-write lithography, techniques were chosen to be compatible with operation of the machine in a lithography mode. Specifically, the beam-defining aperture size and secondary-electron detector placement were not optimum, and techniques such as organometallic decomposition which would cause system contamination were avoided. The most obvious technique for sensing the presence of a logical "zero" or "one" is to utilize voltage-contrast in the secondary electron signal. In particular, if the incident electron beam is directed at a flat aluminum test pad a few microns in diameter, and if the test pad is surrounded by a grounded metal ring several-microns wide, a strong modulation of the secondary electron signal will be obtained as the potential at the test pad is varied from zero volts to a + 5 V logic level. With the test pad at + 5 V, the lowest energy secondaries will not escape from the vicinity of the pad, and the secondary signal will be reduced. Under ideal conditions, a very strong modulation of the secondary electron signal can be achieved and virtually all secondary electrons leaving the pad can be collected. In this ideal case, a high enough signal to noise ratio can be obtained in the secondary signal (with modest incident beam currents) to allow reliable discrimination between a "one" and "zero" logic state with a beam unblank time of less than one microsecond. Thus, in principle, the beam could be deflected to examine more than one million test points per second. Put another way, if a chip were clocked at a 10 kHz rate, 100 selected internal test points could be examined during each clock cycle.

This voltage contrast functional probing should provide excellent testability with minimal area overhead for test points. Unfortunately, results on the LEBES system have been disappointing. Measurements indicate that the secondary electron detector in this system is very poorly placed and receives less than one electron for every ten thousand electrons incident on the sample. For comparison, with a good detector arrangement one could receive about 1 electron for every 10 incident electrons under comparable bombardment conditions. In addition, most of the low-energy electrons collected by the detector appear to be produced in the vicinity of the detector by high-energy electrons backscattered from the specimen which results in a very poor voltage contrast modulation of the "secondary" signal. These two effects reduce the logic level measurement rate to only about 100 Hz. It is anticipated that detector improvements will improve this rate by several orders of magnitude.

A second logic-level sensing technique eliminates most of the difficulties encountered with voltage contrast probing. This technique is capable of logic level sensing at rates of at least 1 MHz, and is free of contamination, charging, and crosstalk effects encountered with voltage contrast techniques. The incident electron probe is pointed at a specially designed test point and is used to select that test point for examination. When an

electron beam penetrates a semiconductor, electron-hole pairs are generated. These electrons or holes can be collected by a p-n junction, causing a current to flow in the integrated circuit. Reasonable incident beam currents might be as large as a few hundred nanoamperes, but such low currents will not appreciably perturb static circuits. However, if an incident electron has a 5-20 keV energy it can generate about 1000-4000 electron-hole pairs. If these are collected by a junction, currents of several hundred microamperes can be induced in the integrated circuit which is larger than the current which is usually supplied by a depletion-mode pullup. In NMOS, since p-n junctions are formed between all n^+ diffused conductors and the substrate, the e-beam can be used to pulldown any diffused conductor to substrate potential, which is usually ground. Thus, by designing so that selected diffused conductors are accessible to the electron beam, it is possible to produce a low logic level at a selected point merely by pointing the electron beam and unblanking it.

This forms the basis for a number of possible sensing schemes including the electron beam controlled multiplexor shown in Fig. 3. In this scheme each of a number of test points (shown as A, B, C...) is connected to the gate of a FET added specifically for test purposes. The drains of these FET's are connected to a test bus which can be the power bus, or a special test bus can be used to reduce the capacitive loading and improve sensing speed. The source terminals of the FET's are left disconnected, and the source-substrate diode provides the electron-beam probed point. If, for example, test point B_T is electron bombarded, the diode will be driven towards forward bias. Depending on the state of test point B, the FET switch will be closed or open and the bombarded diode will be able or unable, respectively, to draw current from the test bus. Thus, the appearance of current on the test bus synchronous with the bombardment of the test point will indicate the logical state. A single wire provides access to many test points with the electron beam providing test-point selection. A number of variations on this basic theme are possible including tree-structured buffered busses. The operation of a single test point will be demonstrated later in this paper.

INPUT INJECTION

Hole-electron pair injection by electron beam provides the basis for applying inputs to a powered-up device without actual input connections. One device, the electron-beam switched latch (ESL), provides a means for applying static inputs to a system under electron beam control. The electron beam is used to control a set-reset flip-flop by bombarding either a set-to-one or a set-to-zero control diode. ESLs can be used to provide stable inputs or clocks, or as volatile control for programmable links during testing.

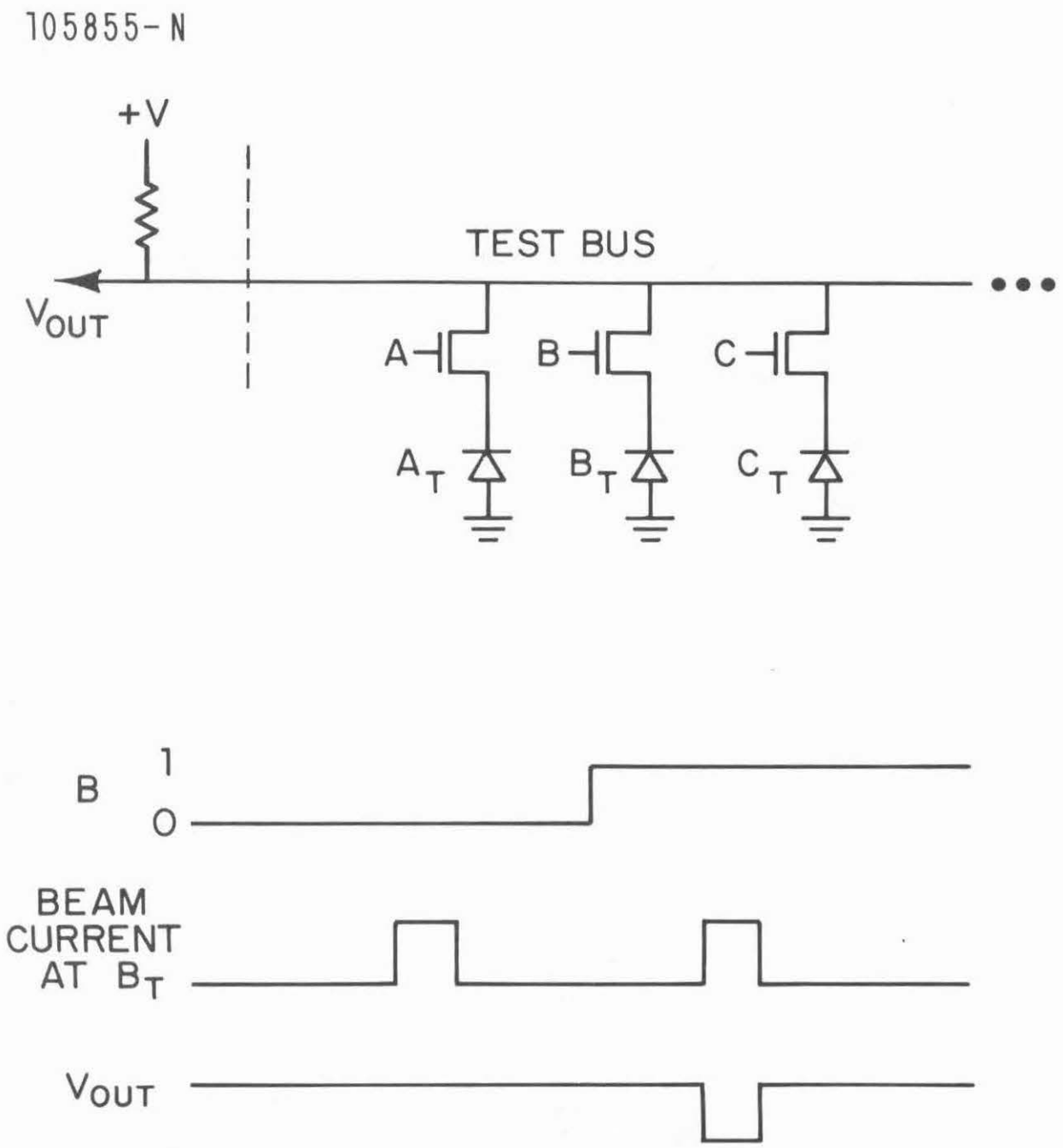


FIGURE 3: A simple electron-beam controlled multiplexor for sensing a selected test point.

Figure 4 is a schematic representation of an electron-beam switched latch. The latch is a pair of cross-coupled inverters with pulldown access provided for the electron beam. Figure 5 shows an actual layout of an NMOS ESL. Electrically-long pullups are used to reduce the required pulldown current to less than 10 μA, and the e-beam pulldown points have been extended well away from the active transistors. Uncovered contact cuts provide electron beam access. This relatively large layout provided many advantages during preliminary experiments, but the ESL could be made as small as two minimum size inverters. Two additional structures are attached to the output of the ESL in Fig. 5. One is an inverter which was added to make the power supply current unequal for the two states of the ESL which made it possible to test ESL operation by simply monitoring supply current. The second structure is a one-bit slice of the electron-beam controlled multiplexor described in the previous section. Thus, this simple chip can provide a feasibility demonstration of combined electron-beam input injection and output sensing.

A chip fabricated at Hewlett-Packard as part of the MPC-580 multiproject chip run was wire-bonded and placed in our ETEC electron beam lithography system. Only two wires, supplying power and ground, are attached to the chip. After setting the beam parameters (5 kV, 7nA) and registering the chip to the electron-beam coordinate system, electron-beam control of the test chip began. As shown in Fig. 6, successful electron-beam switching of the latch and electron-beam probing was achieved. The lower trace in Fig. 6 shows the electron beam x-deflection signal and indicates at which of three locations the beam is positioned. An upwards deflection on this trace corresponds to a leftward motion (in Fig. 5) of the beam. The beam cycles among three positions. From highest to lowest on the trace the positions are set-to-zero, set-to-one, and sense-output. The top trace in Fig. 6 shows turn-on (unblanking) of the electron beam as a small downward blip. The center trace shows an AC-coupled record of the supply current monitored across a small sense resistor. Moving from left to right across Fig. 6, the beam is initially positioned at the set-to-zero location. When the beam is unblanked, the latch switches to zero causing the downward transient in supply current since the latch was designed to draw less current in the zero state. Then, the beam position shifts to the sense location and is again unblanked; no sense pulse appears on the supply current, so the latch is zero. Then, the beam moves to the set-to-one position and unblanks. The immediate change in supply current indicates the ESL has changed state. Finally, the beam is moved to the sense position again and a small pulse appears in the supply current synchronous with the unblanking of the beam. The output is a one. Figure 6 demonstrates complete electron beam control and probing of a small logic circuit, and the principle is extendable to complex systems. The ESL described above could be switched with a 380 ns pulse.

The ESL provides electron-beam control of static logic levels. The electron beam may be used to great advantage in dynamic circuits as shown in Fig. 7. Many NMOS integrated circuits are designed as two-phase clocked, dynamic finite-state machines. A very large number of electron-beam

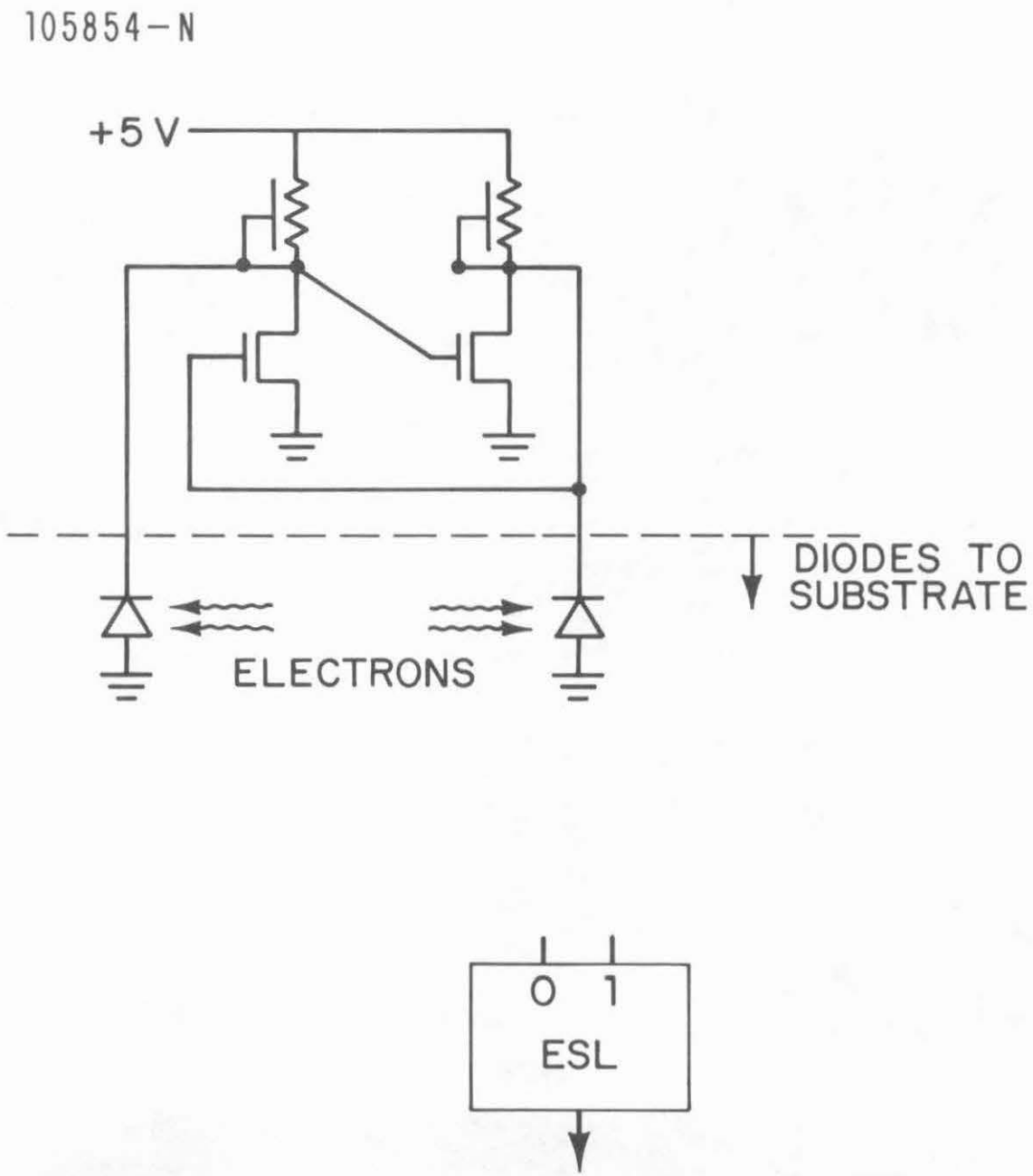


FIGURE 4: Schematic representation of an electron beam switched latch.

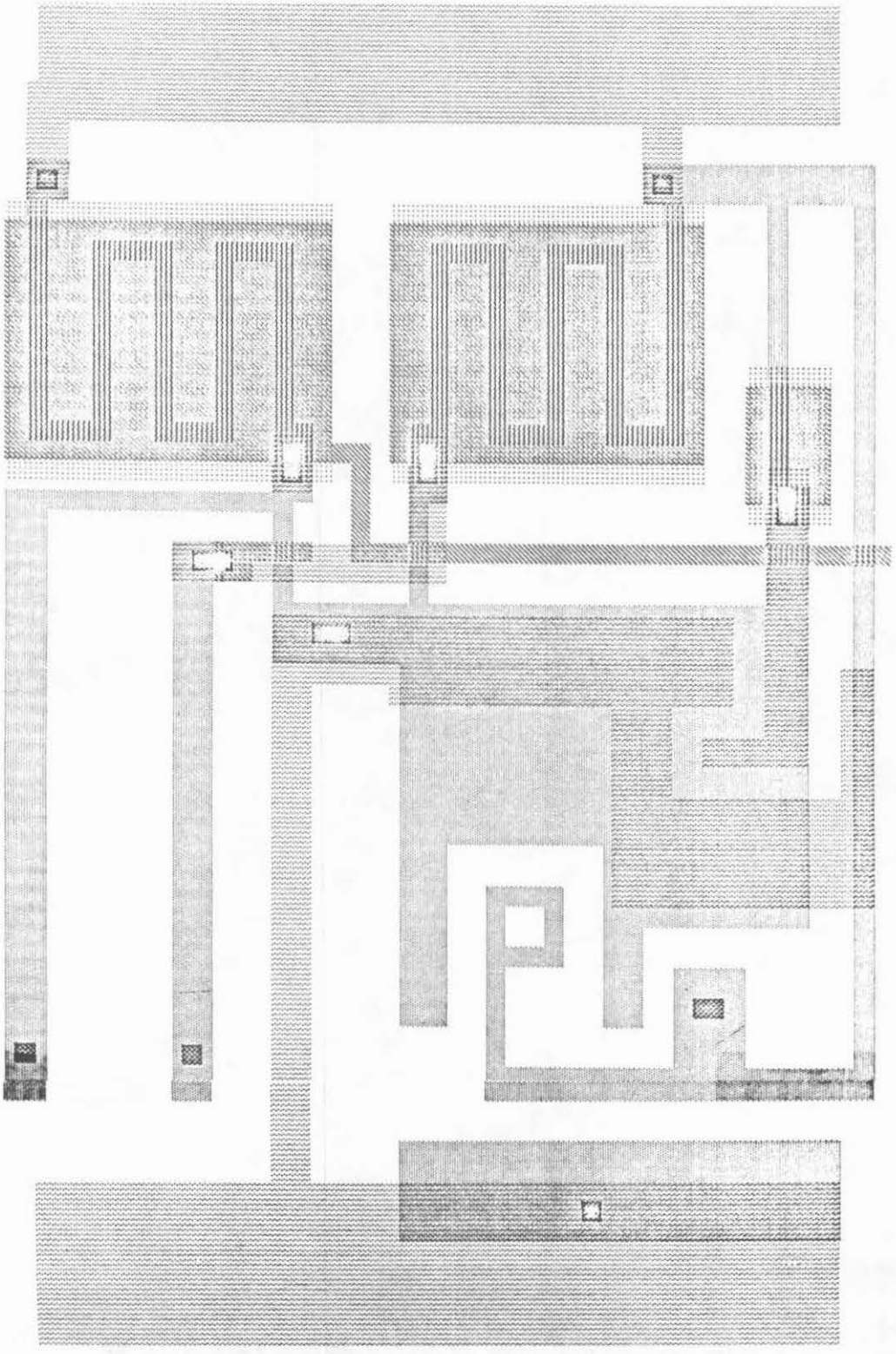


FIGURE 5: NMOS layout of an electron-beam switched latch. Top pad is +5 V and bottom pad is ground. The three dark contact cuts above the ground pad correspond, from left to right, to "set-to-zero", "set-to-one", and "sense" points for the electron beam.

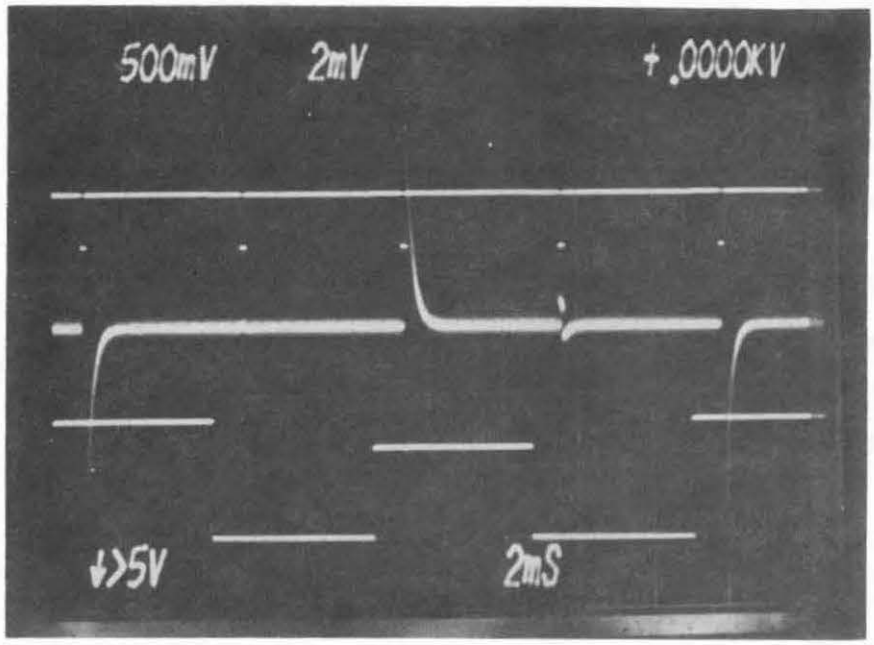


FIGURE 6: An electron beam switched latch in operation. Downward pulses on top trace show beam unblanking. Center trace is AC-coupled supply current to ESL. Lower trace shows beam deflection.

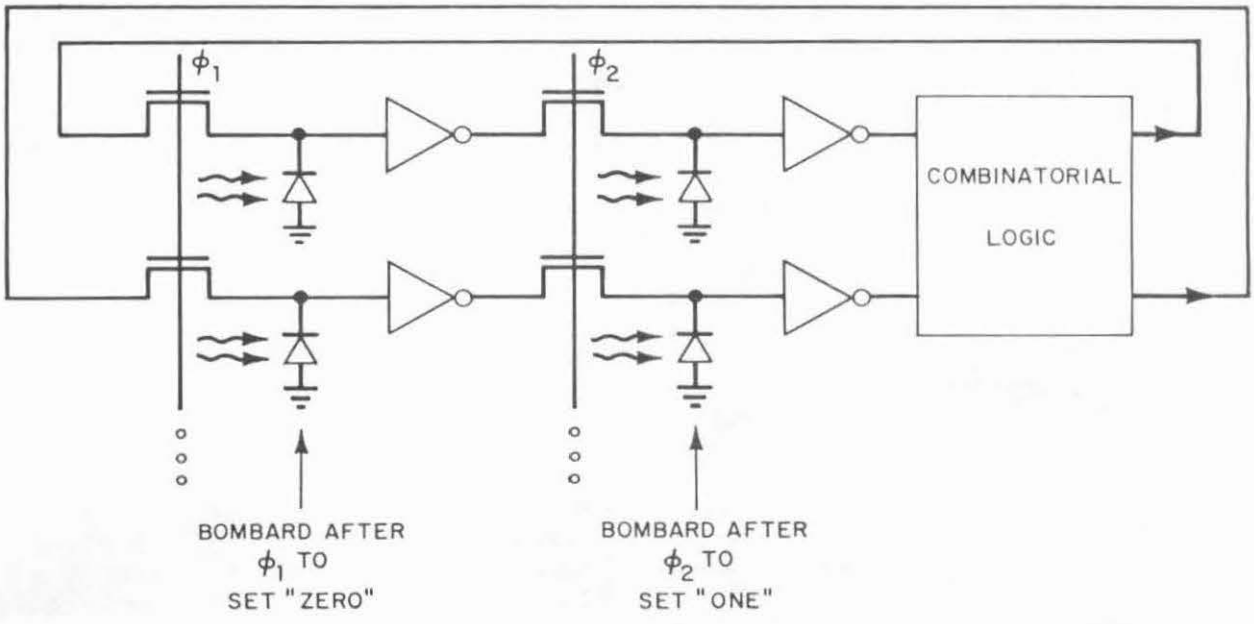


FIGURE 7: A dynamic finite-state machine showing how the electron beam is used to alter the internal state.

accessible test points are available, and the beam is used to selectively dump stored charge after the clock-controlled pass transistors are cut-off. The ability to alter sequentially internal states in the finite-state machine and to probe the consequences will allow an unprecendented degree of testability.

ELECTRON BEAM CONTROL OF NON-VOLATILE SWITCHES

The ability to open and close selected switches on the wafer is essential if one wishes to customize subsystems and modify interconnects. Ideally these switches should be easily flipped from on to off (and vice-versa) under e-beam control and should exhibit high off resistance and low on resistance. Once programmed by the beam they should retain their state indefinitely. Two types of electron-beam alterable switches, field-oxide FETs and floating-gate FETs, are described below.

The field oxide FETs are parasitic devices present in all NMOS processes. When a polysilicon or metal conductor runs over thick field oxide, a parasitic FET is formed between adjacent diffused conductors. Normally, this FET is off since the combination of thick oxide and field implantation raises its threshold to many volts. Electron-beam irradiation of oxides with a bias applied across the oxide can result in a large buildup of positive charge in the oxide, presumably due to hole-trapping. Specifically, if a positive voltage is applied across thick oxide and the FET is irradiated a thin layer of positive charge will accumulate near the silicon surface producing an effect equivalent to applying the bias across a thin oxide of only about a hundred angstroms thickness. Since this charge remains trapped in the oxide after the irradiation and bias are removed, a large (> 50 V) negative threshold shift is induced in the FET. For example, a polysilicon gate field-oxide FET formed in the MPC-580 run exhibited a threshold of > 10 V. Thus, for normal logic levels between 0-5 V, the gate cannot turn-on the FET, and adjacent diffused conductors are not connected. This FET was strongly turned on by applying + 3 V to the gate and irradiating the gate oxide. As shown in the top of Fig. 8, the FET is strongly turned on after e-beam irradiation with a positive gate-programming voltage. The four closely spaced characteristics correspond to gate voltages of 0, 1, 2 and 3 V indicating that the FET is strongly on regardless of the gate voltage after programming. By biasing the gate at zero volts and irradiating again, the FET can be turned off. The lower half of Fig. 8 shows the drain-source characteristic of the FET after this operation. For gate voltages varying from 0-5 V, the FET is off.

E-beam programmed field-oxide FETs provide a simple, reprogrammable element for restructuring and customization. The voltage applied to the programming gates during electron beam bombardment can be generated locally from the output of an ESL or can be supplied over a single programming wire such as the power bus. The retention time of the on state is at least a few weeks for devices operated at room temperature, but the retention characteristics are likely to be poor if the devices are operated at 150°C for even short periods. Nonetheless, this e-beam controlled switch should be very

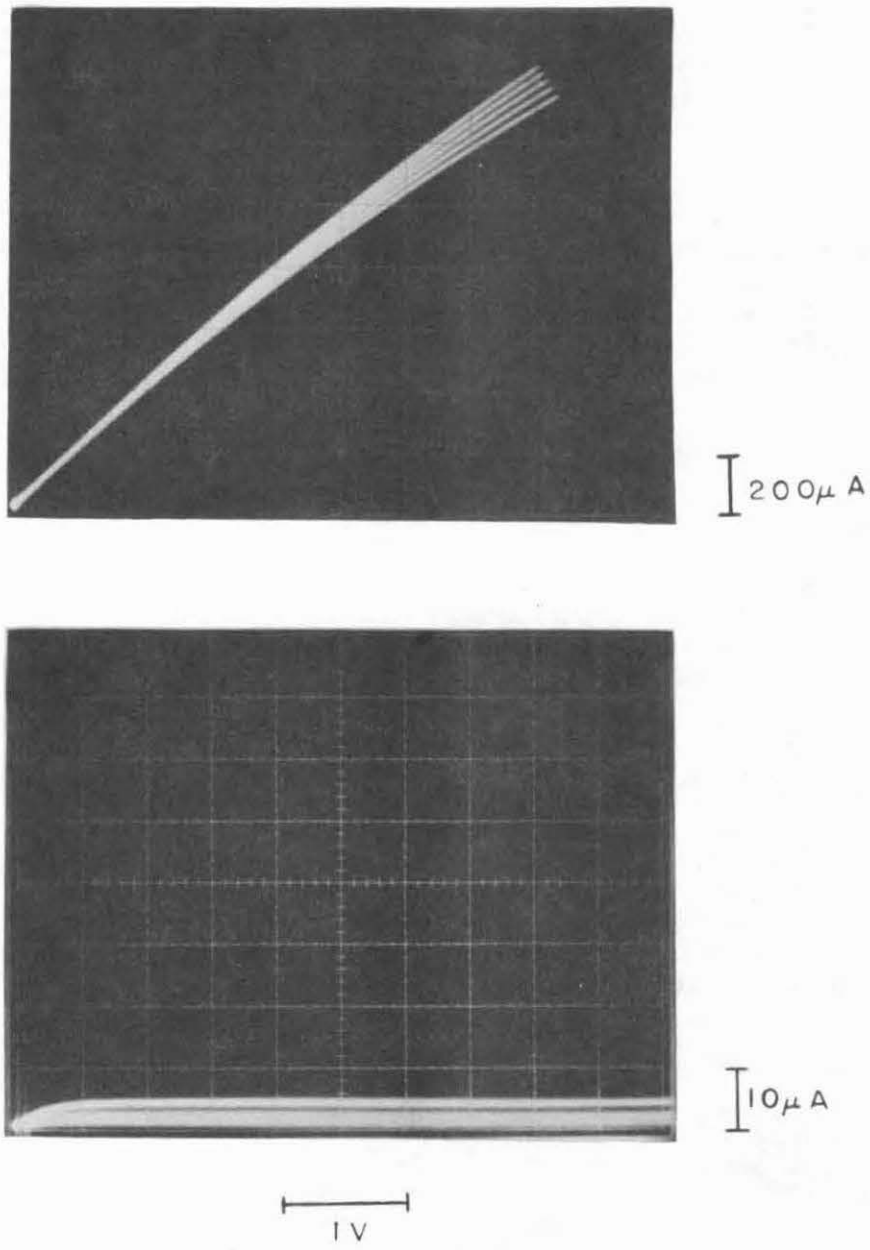


FIGURE 8: A field-oxide FET non-volatile switch after e-beam programming. Switch is initially off. Top picture shows FET characteristic after e-beam programming to the "on" state. Note the low sensitivity of the FET conductance as the gate voltage is varied from zero to +3 volts. Bottom picture shows "off" state after e-beam reset.

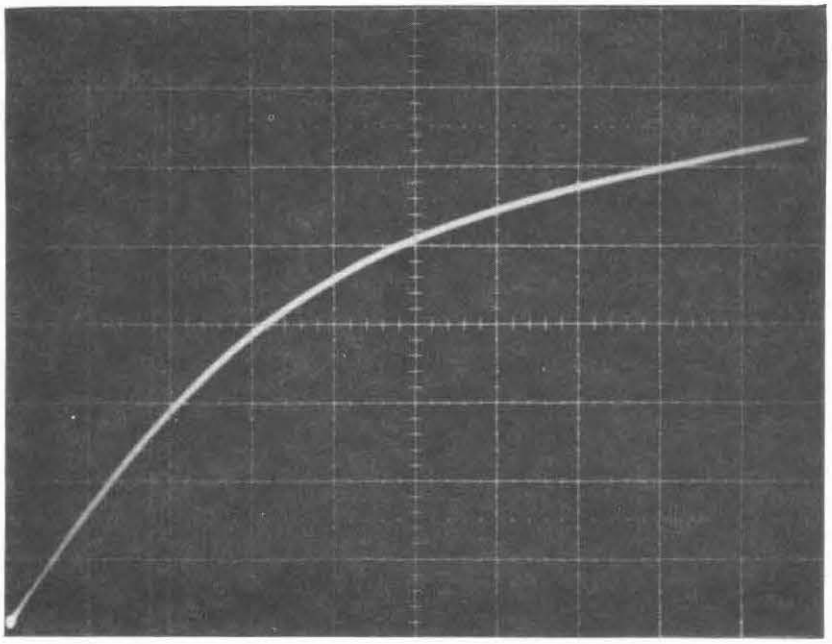
useful if the devices are operated at liquid nitrogen temperatures, and will certainly prove to be a useful element in laboratory studies of large-scale restructurable systems. Less than 1 $\mu C/cm^2$ of 20 kV bombardment is required to produce the threshold shifts, and a programming time of less than 1 μs per switch is possible.

Electron beam programmed floating gate FETs should provide a reliable, truly non-volatile switch. Electron storage on floating gate FETs is the basis for information retention in UV-erasable EPROMs which have enjoyed wide commercial acceptance and have excellent retention characteristics. FAMOS[9] electrically-programmable ROMs are programmed by hot-electron injection through the thin gate oxide where the hot electrons are generated by avalanche breakdown of the drain-substrate junction. Electron-beam programming of floating gate devices is possible if an electron beam is directed at an oxide-covered gate, causing electrons to penetrate the oxide and become trapped on the gate. The trapped electrons will charge the gate to a negative potential.

Some preliminary experiments have been performed on depletion-mode floating gate devices fabricated as part of MPC-580. These devices were normally on, and could be turned off by electron bombardment of the gate. Figure 9 shows a drain-source characteristic for a FET before (top photo) and after (bottom photo) electron-beam programming. At a 5 V drain-source bias, the current is 100 times greater in the on state than in the off state. The residual current of 5 μA in the off device was determined to be the result of formation of a weak buried channel in the depletion mode device. Biasing the substrate to -0.4 V increased the on : off ratio to better than 10000 : 1. A slight modification of the depletion mode implant would greatly reduce the magnitude of the buried channel. The large floating gate devices used for these experiments required 370 μs to insure complete turn off using a modest 2 nA beam. By using larger beam currents and smaller devices, programming times of a few microseconds could be achieved.

CONCLUSION

Control of the state of a simple NMOS integrated circuit using an electron beam has been demonstrated. Techniques have been demonstrated for input injection, output sensing, and programming of non-volatile switches using a commercially-available electron beam lithography system and conventional NMOS technology. Many of the techniques for input injection and output sensing have also been demonstrated using light beams, but the experimental apparatus was very limited. Though many approaches to "scanning-beam" probing and restructuring are feasible, the state-of-the-art in electron beam deflection, blanking, etc., is highly advanced, and electron beam probing and restructuring could be a reality in the very short term. This can provide us with a flexible tool to understand the problems in constructing wafer-scale systems.



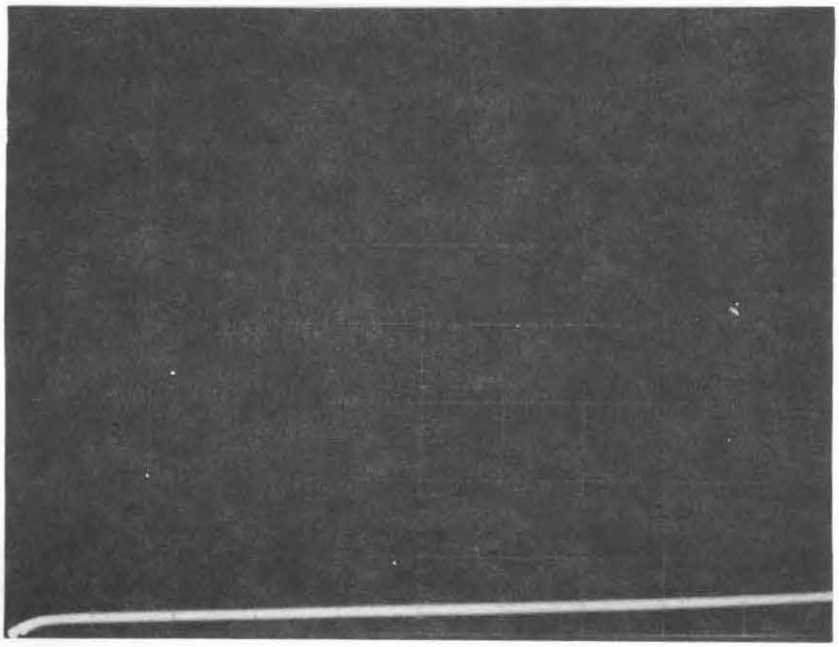


FIGURE 9: A depletion-mode floating gate FET before (top photo) and after (bottom photo) electron beam programming.

ACKNOWLEDGMENTS

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