FAST TURNAROUND FABRICATION FOR CUSTOM VLSI

Gunnar A. Wetlesen
VLSI Technology, Inc., Santa Clara, California

Now, you are probably wondering how somebody on crutches is going to be able to provide fast turnaround or anything. Well, excuse me while I grapple with everything that I have to carry up here.

While we are in an informal mode, I would like to say that we made an acronym of an acronym, and we go by VTI, standing for VLSI Technolgy Inc.

The so-called foundry concept as first proposed by Carver Mead is one of the areas of business that VTI hopes to support. I am not sure if our coming about was to make Carver's prognostications accurate, or whether it is indeed a reflection of the support that we have gotten from a number of investors. I would like to acknowledge them. There is a computer company with vision and venture capitalists that are represented in the audience today that made VTI come about. Previously, the idea of the foundry was only available internally in large corporations, such as Hewlett-Packard, who did the prototyping work for the MPC runs that Lynn Conway described earlier. We are going to be one of the factors in that area in the future.

So, beginning with the more formal portion of this talk, I will be addressing the whole area of custom VLSI, and addressing the MPC area just a little bit.

The use of custom and semi-custom circuits is rapidly growing in many electronic equipment areas, particularly as the potential of VLSI is being realized. Helping create this intensity in custom activity are the following advantages available through customization seen in contrast to the use of standard products:

1) A competitive advantage -- product differentiation and/or proprietary feature sets.

2) A performance advantage -- reduced component count and associated system overhead.

Realizing the potential of custom VLSI circuits is analogous to the emergence of the microprocessor a decade ago. In this case it is presently limited by the front-end design phase (both schedule and cost). Thanks to many of the people present here today, the design mechanism for translating systems into silicon is evolving rapidly.

Regardless of the design mechanism or the driving force toward custom in terms of systems advantages, all custom circuits must subsequently navigate the same obstacle in development: the time-consuming and often iterative prototyping phase.

Fast turnaround for custom VLSI fabrication will now be examined. This fabrication need will be translated into terms of the characteristics desired of the MOS/IC manufacturer. We believe there is a need in the semiconductor industry for new kinds of companies properly postured to service the requirements for the coming era of custom VLSI.

Fast turnaround for custom VLSI fabrication as a goal defines three general requirements which must be supported for the goal to be met. They are:

1) VLSI level of fabrication technology.

2) Supporting custom designed circuits (as opposed to standard products).

3) Providing fast turnaround fabrication.

Let us consider now each of these in detail and the resulting "factory" characteristics in terms of operating philosophy, organization, equipment, and people.

VLSI FABRICATION TECHNOLOGY

There are several common definitions of what is VLSI. While best defined in terms of system complexity, other definitions are often based on feature size or device complexity. For example, the state-of-the-art 64K dynamic memory has been referred to as a VLSI chip by virtue of its greater than 100,000 transistor count (figure 1). Certainly, the domain of logic circuits above 10^5 transistors can be associated with VLSI system complexity.

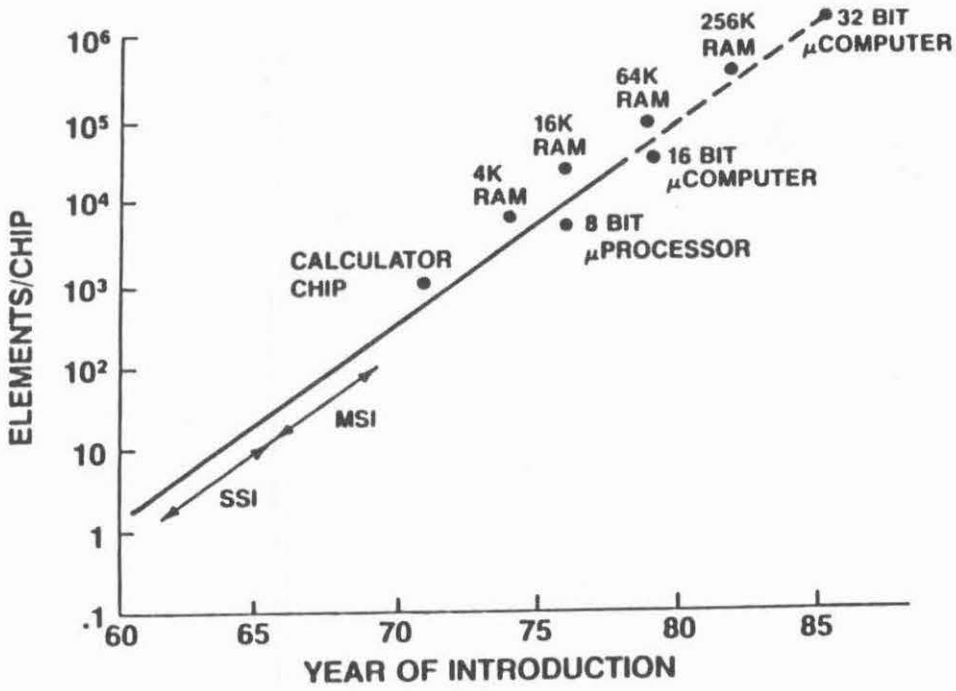

Figure 1

What kind of fabrication technology for VLSI? as a practical matter, fabrication processes will evolve with time. Current technologies with VLSI potential included scaled n-MOS (commonly called H-MOS) and oxide isolated CMOS. One thing that is clear is that process technologies are becoming more

specialized depending on their application (figure 2). For example, in memory technology, double poly and diffused capacitors have been evolved to optimize the density of dynamic RAMs whereas static RAMs have incorporated high value polysilicon transistors and multiple transistor thresholds for both density and performance. I think it can be concluded that evolution of technology for VLSI custom circuits will be on a different branch of the technology tree compared to memory circuits. In particular, the use of multilevel metal as a solution to the interconnect and signal delay problem is overdue for logic circuits. Additional benefits would be gained by features improving ROM and PLA densities.

SPECIALIZATION OF PROCESS TECHNOLOGY

PRODUCT TYPE	SPECIAL PROCESS FEATURES
DYNAMIC RAMS	• DOUBLE POLY • ENHANCED CAPACITORS
STATIC RAMS	• DOUBLE POLY (INTERCONNECT) • POLY LOAD RESISTORS
ROMS	• SELF-ALIGNED CONTACTS • MULTIPLE THRESHOLDS
LOGIC CIRCUITS	• MULTILEVEL METAL

Figure 2

In terms of commercial state-of-the-art equipment, the current noncaptive lines are still based on 1:1 projection aligners. Selective use of direct wafer steppers on certain critical mask levels is being employed for manufacture of volume standard products. Due to the logistics and the potential for repeating defects associated with changing 10x reticles, the use of 1:1 projection printers is favored for producing lower volume custom and customizable circuits. With use of planar plasma etching and reactive ion technologies, resulting average feature sizes of 2-3 microns appear readily manufacturable with projection aligners in the near future (figure 3). Other aspects of equipment selection will be considered later.

MOS COMPLEXITY/DIMENSION FORECAST

YEAR	DEVICES PER CHIP	DIE SIZE (mils)	AREA (mils²) PER DEVICE	LINE WIDTH
1978	35,000	200 x 200	1.26	4μ
1982	250,000	300 x 300	.36	2.1μ
1985	1,000,000	400 x 400	.16	1.4μ

Figure 3

SUPPORTING CUSTOM CIRCUITS

Supporting custom circuit manufacture is markedly different than the merchant IC industry supplying standard products. The first and most obvious characteristic is that a custom circuit is by nature unique. This uniqueness begins with the generation of the mask set, and involves both a significant data transfer of the base description of the circuit layout, and also the practical details of mask geometry polarity, and skewing, and process monitor chip insertion. The industry needs to develop clean, automated procedures for easy customer interfacing.

The first step is to replace the personal phone call and the physical transfer of data base tapes, which will be accomplished instead by what we call "VTI Net." Access to VTI via a commercial computer network allows the transfer of design files in CIF and other formats (figure 4). More importantly, an inquiry service will be established to answer the basic questions a designer in a remote location needs to ask in order to interface with our fabrication service, including cost and scheduling information as well as formats, etc.

NETWORK ACCESS TO VTI ("VTI NET")

- VIA COMMERCIAL NETWORK
- ACCEPTS DESIGNS IN CIF (AND OTHER FORMATS)
- ALLOWS FOR BASIC INQUIRY RESPONSE SERVICE

Figure 4

Central to such an arms-length service working are standardized interfaces before and after fabrication (figure 5). In particular, the technology and design rules must be common. nMOS based on lambda rules will be offered

STANDARDIZED PRE-FABRICATION INTERFACE

- BASED ON LAMBDA DESIGN RULES
- REQUIRES E-BEAM MASK GENERATION
- "STARTING FRAME" INSERTED BY VTI

Figure 5

plus specials on a "non-network" basis (figure 6). Mask generation will be done using an electron beam system not only for dimensional and complexity reasons but also because it greatly simplifies the starting frame task. Alignment keys and critical dimension measurement points need not be inserted on the circuit as those are included within the process control monitor (PCM), chip inserted by VTI in the mask set.

CUSTOM INTERFACES

TOOLING	• DATA BASE • MASKS
FABRICATION	• VERIFICATION • SPECIAL PROCESSING
TESTING	• WAFER LEVEL • PACKAGE LEVEL

Figure 6

This same PCM serves as the common denominator for evaluation of the processed wafer lot (figure 7). It provides process parametric characterization data automated in both measurement and data reduction. VTI intends to

STANDARDIZED POST-FABRICATION INTERFACE

- **PARAMETRIC CHARACTERIZATION VIA PROCESS CONTROL MONITOR (PCM)**
- **RESULTS OF "CANARY" CIRCUIT EVALUATION (OPTIONAL YIELD DATA)**
- **PROTOTYPE PACKAGING (FOR CHIPS MEETING VTI ASSEMBLY STANDARDS)**
- **ARCHIVAL OF PCMs (FOR OPTIONAL RELIABILITY AND OTHER EVALUATIONS)**

Figure 7

take advantage of NBS work and to make this PCM and support documentation widely available to provide a standard suitable for multiple sourcing of fabrication services. The PCM will provide, however, only limited information in terms of yield analysis. In addition, VTI will include a "canary" circuit, for example a large shift register, whose functionality will be part of the wafer acceptance criteria. In early prototyping phases statistically significant quantities of these test circuits can be incorporated into the mask set for correlation and projection of both yield and circuit performance. The PCMs will be saved in die form when a packaged chip rather than wafer level interface is employed, so that they can be used both for later electrical characterization and for quality and reliability verification for military programs. Similarly, correlation with performance of both the prototype circuit and the "canary" will be even more valuable if process variants or "tweaks" are employed either to give special features (such as on-chip analog interfaces) or to give performance enhancements.

In addition, the "VTI Net" will also be set up with multiproject chip (MPC) capability in mind, similar to that described earlier by Lynn Conway (figure 8). Initially, the MPC capability will be used internally to support VTI's design courses. Based on a core of material available on video tape, these courses are being given in remote locations for appropriately equipped companies which will in turn enjoy MPC availability.

FUTURE MPC CAPABILITY PLANNED

- **INITIALLY INTERNAL FOR VTI COURSES**
- **INTERIM AVAILABILITY ON A SELECTED CUSTOMER BASIS**
- **NETWORK CAPABILITY IN FUTURE (LOGISTICAL, TECHNICAL AND PROPRIETARY ISSUES)**

Figure 8

In the future, the courses will be given at VTI's planned design center. When technical and proprietary issues are solved, the MPC capability will be expanded and will become available for routine prototyping on an individual basis via the network.

Let us now consider the workings of the factory which supports the fabrication of custom VLSI. As a result of the percentage of prototype runs and the larger number of unique mask sets being run to get suitable volumes in a given manufacturing module, the support organizations of a custom circuit factory must be substantially different than current merchant IC suppliers. The greater logistics task begin with order entry, where a technical transfer is implicit, and continues through the factory with production control, quality assurance, and other organizations being matched accordingly. Clearly, the task of performing on a build-to-suit basis at each step from maskmaking through fabrication, test, and assembly, while maintaining a line item orientation, is much greater than that for the inventory orientation used in standard products. The operating philosophy completely different, perhaps best described as the need to be effective rather than efficient, especially in the context of fast turnaround. The caliber and awareness of people in these support organizations must be matched accordingly. The mainstay of their equipment must be real time control systems for scheduling and tracking programs throughout the factory cycle. Ultimately, status information should become available as part of the inquiry service over the network.

PROVIDING FAST TURNAROUND

In traditional IC companies, factory production cycles of 16 weeks, assuming mask availability, are not uncommon. Of this cycle typically 6-8 weeks is in wafer fabrication. Clearly, this cycle is untenable for circuit prototyping -- a year could be consumed in 2-3 iterations. As will be seen, however, carryover of a fast turnaround philosophy into production also brings tangible benefits.

The theoretical limit on fabrication cycle time of a typical MOS process is on the order of 2-3 days. A practical goal for minimum lot size fabrication of prototypes is one week if the factory is organized accordingly to minimize waiting in queues before each operation. The preeminent requirement in achieving fast turnaround is the operating philosphy (figure 9). Instilling in the work force the concept that "minutes count" is a further

COMPANY CHARACTERISTICS

COMPARISON	EXISTING IC CO's	PROPOSED CO
GENERAL ORGANIZATION	BASED ON EFFICIENCY	BASED ON EFFECTIVENESS, PERFORMANCE TO SCHEDULE
PHILOSOPHY	INFLEXIBLE	FLEXIBLE (PROCESS, PRODUCT, ETC.)
	COST BEFORE SERVICE	SERVICE ORIENTATION
	PRODUCT ORIENTATION	CUSTOMER ORIENTATION
	INVENTORIES COUNT	TIME COUNTS

Figure 9

development of this theme. In addition to the scheduling and tracking organizations operating as a "real time" function, the other organizational strategy for providing fast turnaround of prototypes is the pilot line concept (figure 10). Located within the manufacturing facilities to assure ease and success of later production transfer, a prototype pilot line can, by providing the necessary focus and priority, reduce fabrication cycle times severalfold. In addition to providing an elite team of skilled people, it is necessary to give last-in, first-out priority on shared equipment plus provide dedicated equipment at steps where lot uniqueness is maintained, such as photomasking. Furthermore, factory equipment must be more redundant to provide capacity for "surge conditions" and be chosen to be not too "state-of-the-art" so as to maintain high up-time.

CYCLE TIME COMPARISON

I PROTOTYPES

STEP	TYPICAL	POSSIBLE
MASK MAKING	4—6 WEEKS	3 DAYS
WAFER FAB	4—6 WEEKS	9 DAYS
PACKAGING	2—3 WEEKS	3 DAYS
TOTAL	10—15 WEEKS	3 WEEKS

II PRODUCTION (WITH EXISTING MASKS)

TYPICAL	POSSIBLE
12—16 WEEKS	6—8 WEEKS

Figure 10

Wafer fabrication is only one link in the turnaround chain. Mask making and assembly are others. In-house control of an e-beam mask generation system can keep this cycle time minimized. Typical writing and processing times make one plate per hour realizable with additional time for inspection. As a result, two- to three-day turnaround for a mask set is practical while still providing priority for single layer redos or customized devices. Similarly, an in-house prototype packaging line can assemble prototypes in a couple of days.

Summing up these individual times it can be seen that less than a week total cycle time from receipt of tapes to custom prototypes could be routine if an IC manufacturing facility were postured as described. Moreover, the production cycle times could easily be halved compared to traditional IC suppliers in this same atmosphere. In terms of limiting exposure to upstream yield or reliability problems as well as responding to increased customer needs, shortening of the manufacturing pipeline is an equally attractive possibility.

CONLUSION

VTI has been funded to serve the need of a high technology for VLSI and a service-orientation to provide quick turnaround.