CONSIDERATIONS FOR AN ANALOG FOUR QUADRANT SC MULTIPLER

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ABSTRACT

This paper outlines the considerations and design of a four quadrant analog multiplier using switched capacitor (SC) techniques. The design algorithm for accomplishing the multiplication is described. Implementation of the algorithm is then presented. The predicted accuracy of the multiplier is given and compared to preliminary breadboard measurements. The multiplier described is presently being fabricated as an integrated circuit on a university multichip project using double-poly MOS technology.

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INTRODUCTION

Practical analog signal processing using integrated circuit technology has been made possible by the application of SC techniques.[1] The accuracy of analog signal processing systems can approach 0.1% which is equivalent to approximately 10 bits of digital information.[2] The primary analog signal function which has been implemented using SC techniques is the filter.[3] Some non-filter applications have also been considered such as oscillators,[4] diodes,[5] and digital-to-analog converters.[6-9] Some work has been done in the area of modulators,[10] but little if any consideration has been given to a true analog multiplier.

The objective of this paper is to take the proven techniques of SC circuits and apply them to the development of a four-quadrant SC multiplier. The result is a very useful analog signal processing component which is compatible with MOS technology. The speed of such a multiplier would not be expected to match the integrated bipolar analog four-quadrant multipliers presently available[11] because of the use of sampled data techniques. Preliminary results show that it is possible to eliminate many of the multiplier errors and to avoid the extensive fine tuning and external components that must accompany the use of bipolar analog four-quadrant multipliers. One useful technique that can be accomplished in SC circuits is to sample the offsets and cancel their contribution during the next clock phase period. This technique is considered as a means to reduce the errors associated with the analog, SC multiplier.

The paper will first consider the principles of operation by which the SC multiplier will be designed. These principles of operation will then be used to develop an implementation of the multiplier. An analysis of this implementation will provide the predicted performance which will be compared to breadboard results. This will be followed by the present status of this development and the future steps that will be taken. Brief consideration will be given to the implementation of

this multiplier using MOS technology which is presently under construction.

PRINCIPLE OF OPERATION

In seeking a multiplier compatible with MOS technology, one might ask why not simply replace the bipolar junction transistors in the bipolar multiplier with MOS transistors. In theory, this approach proposed by the question should work. However, in practice there are several problems. The bipolar multiplier works on the principle of current ratioing using the transconductance of the bipolar junction transistor. Unfortunately, the MOS transistor has much lower transconductance and larger offset voltages leading to a four-quadrant multiplier having large errors. While the transconductance of the MOS transistors could be increased by using very large devices, the offset voltages would create too much error. With the concepts of SC circuits in mind, a new approach was sought which would take advantage of the SC methods to provide improved performance.

The operating principle chosen for the MOS multiplier can be explained by the block diagram in Fig. 1. This block diagram is used to represent the multiplier which will be designated as the operational multiplier. The operational multiplier has three inputs and one output. Two of the inputs are designated as multiplicands and the third input is called the divisor. The principle of operation can be simply stated as follows. Operate simultaneously on one of the multiplicands and the divisor in such a manner that the divisor is equal to the remaining multiplicand times a constant. For example, suppose that the operated value of the divisor C is equal to the multiplicand B and is given as

$$\text{Operated value of } C = KC = B \tag{1}$$

If the remaining multiplicand, A, is operated on in the same manner as

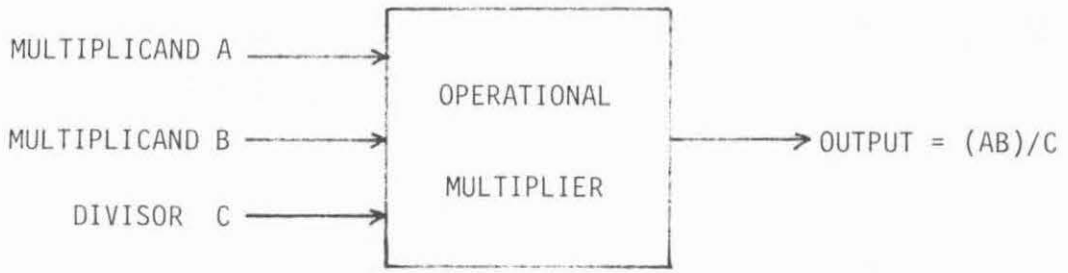


Fig. 1 - Block diagram of an operational multiplier.

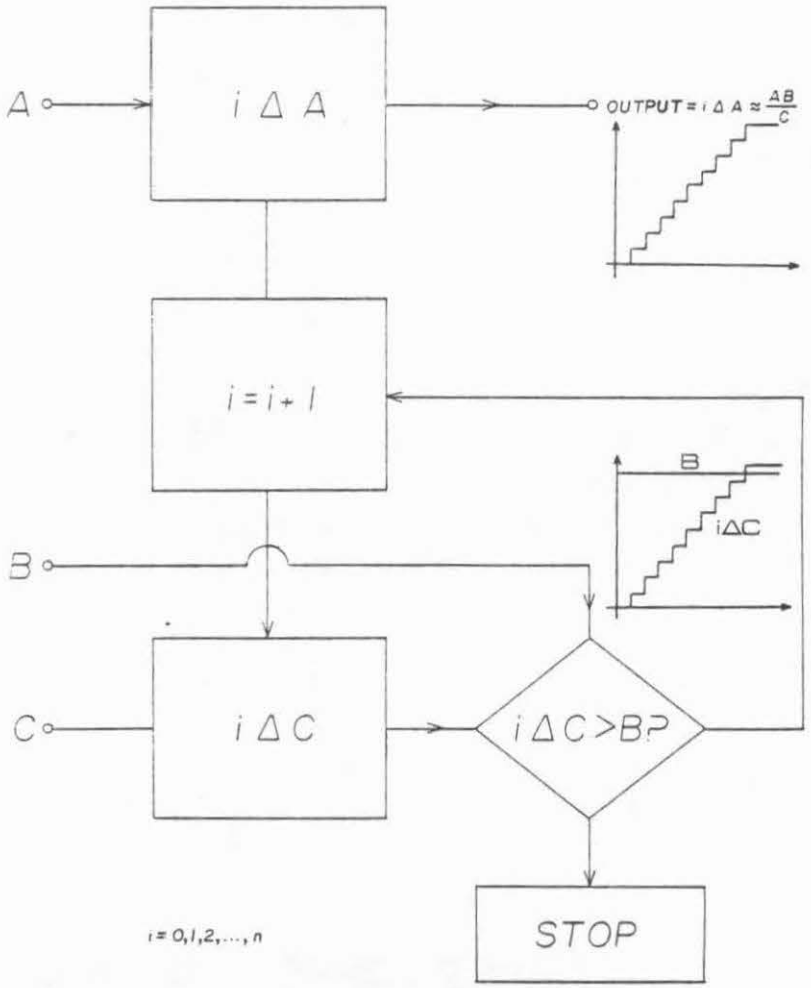


Fig. 2 - Counter implementation of the operational multiplier.

the divisor C then we can write

$$\text{Operated value of A} = KA \tag{2}$$

From (1) we see that $K = B/C$. If the output is equal to the operated value of A then the output can be expressed as

$$\text{Output} = \text{Operated value of A} = (AB)/C \tag{3}$$

If the output of the operational multiplier is equal to the operated value of A, then multiplication between the inputs A and B has been achieved. We also note that division of the product (AB) by C has also been achieved. Although the operations indicated above can be more complex than multiplying by a constant, this choice has the advantage of simplicity and is used in this paper.

IMPLEMENTATION

The first implementation for analog multiplication to be considered was the counter approach as shown in Fig. 2. This approach is an obvious implementation of the operational multiplier. The counter approach consists of two accumulators designated as $i\Delta A$ and $i\Delta C$. These accumulators continue to add ΔA and ΔC until $i\Delta C$ is larger than B.

Once the accumulation stops, it is seen that B is equal to $n \Delta C$, or at least within one unit of Δ. Obviously one can see that in order to achieve high accuracy the incremental constant, Δ, must be very small. The problem arises in that as Δ decreases, the number of steps, n, increases. If B is much greater than $\Delta \cdot C$, then a long interval will be necessary to obtain the output signal. The disadvantage of this approach is that the operation can take too much time, particularly if B is much greater than ΔC.

The second method selected is the successive approximation approach as used in analog-to-digital converters, and is shown in Fig. 3. One can readily see the advantages of this approach over the previous one.

The master accumulator successively approximates the value of V_B resulting after n steps in

$$\sum_{i=0}^{n} \frac{b_i}{2^i} V_C \cong V_B \tag{4}$$

Rearranging terms:

$$\sum_{i=0}^{n} \frac{b_i}{2^i} \cong \frac{V_B}{V_C} \tag{5}$$

But,

$$V_{out} = \sum_{i=0}^{n} \frac{b_i}{2^i} V_A \tag{6}$$

Substituting,

$$V_{out} \cong \left(\frac{V_B}{V_C}\right) V_A \cong \frac{V_A \cdot V_B}{V_C} \tag{7}$$

Eq. (7) is approximate to within 2^{-n} times V_C. This difference between eq. (3) and eq. (1) can be reduced by increasing the value of n. One can see that the successive approximation approach converges to the proper value much faster than the counter approach.

It turns out that this method is naturally adaptable to SC circuits and requires only three matched capacitors to implement the basic accumulator operation. Fig. 4 shows a circuit which resembles a SC integrator but has been modified for our purposes in implementing eq. (3). The circuit works as follows. At the beginning of the multiplying operation, the left-hand capacitor C is charged to the voltage V_C. The right-hand capacitor C is completely uncharged during this time. The multiplication operation begins by switching across both capacitors by exactly one-half. The value of $V_C/2$ is then applied either positively or negatively to the capacitor C connected around

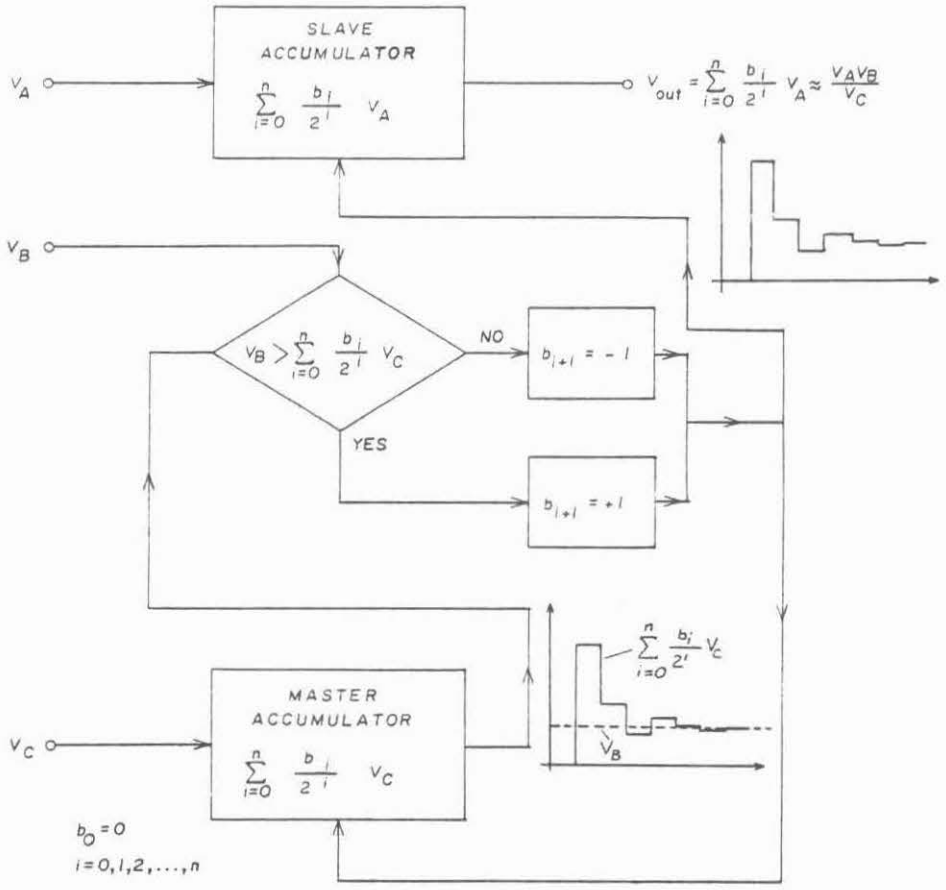


Fig. 3 - Successive approximation implementation of the operational multiplier.

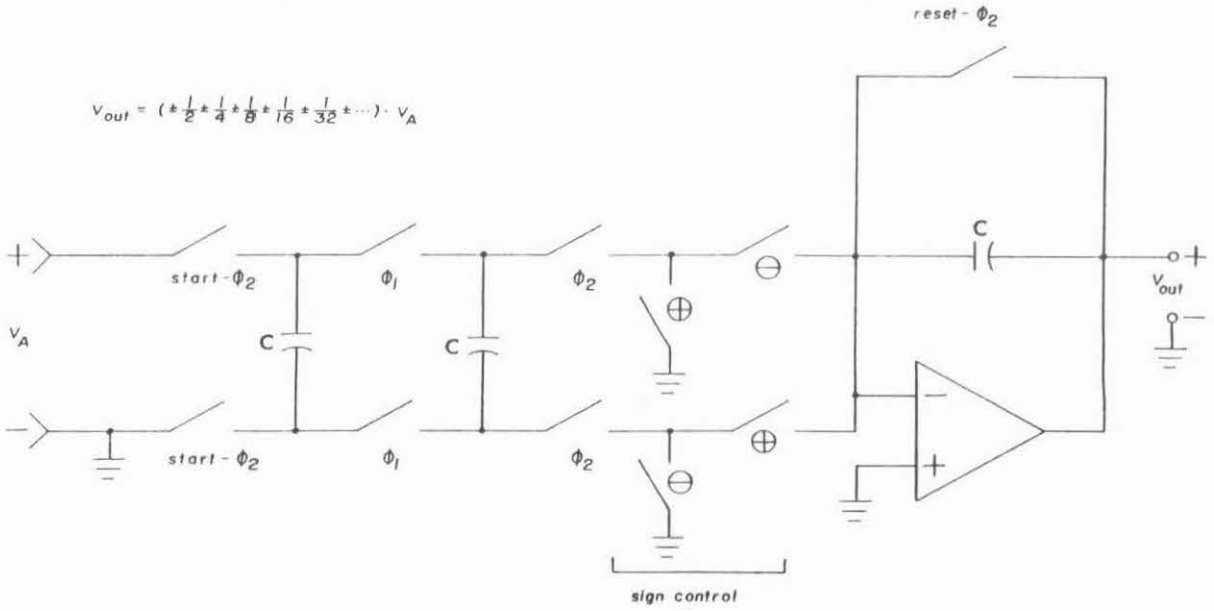


Fig. 4 - Switched capacitor accumulator circuit.

the op amp. This capacitor serves the purpose of a memory or an accumulator. The decision to accumulate in a positive or negative manner is made by comparing the output of the master accumulator with a reference voltage. If the accumulator is below this voltage, then the next sample is added to the accumulator. In this manner, the accumulator successively builds in value KV_C which approaches the reference voltage. A second accumulator operates on V_A in the same manner as the first accumulator resulting in the implementation of eq. (3). Since the accuracy of the accumulators is dependent upon how well the three capacitors designated as C can be matched, each sample of V_A should be transferred to the accumulator with an error of less than 0.1%.

Fig. 5 shows the implementation of the four-quadrant multiplier using the successive approximation accumulator of Fig. 4. The accumulators use a set of switches indicated as "+" and "-" to determine the polarity of the accumulation. In the "+" position the accumulator has the advantage of operating in a stray-sensitive mode which prevents capacitor and switch parasitics from affecting the accumulation.[12] In the negative position the accumulator is unfortunately susceptible to these parasitics which must be taken into account when considering the accuracy of the circuit. Note that the sign of the four-quadrant multiplier is automatically determined in Fig. 5. This is possible because the accumulators are bidirectional.

A shift register is used to control the operation and sequencing of the multiplier. The first output of the shift register is used to reset the accumulators by discharging the accumulation capacitance, and by charging the left-hand capacitor C to the value of V_A (or V_C). The accumulation process continues until the shift register reaches the point where the sample-and-hold circuits are triggered and C is reconnected to the voltage V_A (or V_C). The theoretical accuracy of the multiplier will be determined by the number of steps taken in the successive approximation sequence. Obviously, if no other considerations are pertinent, the accuracy times speed of performing a

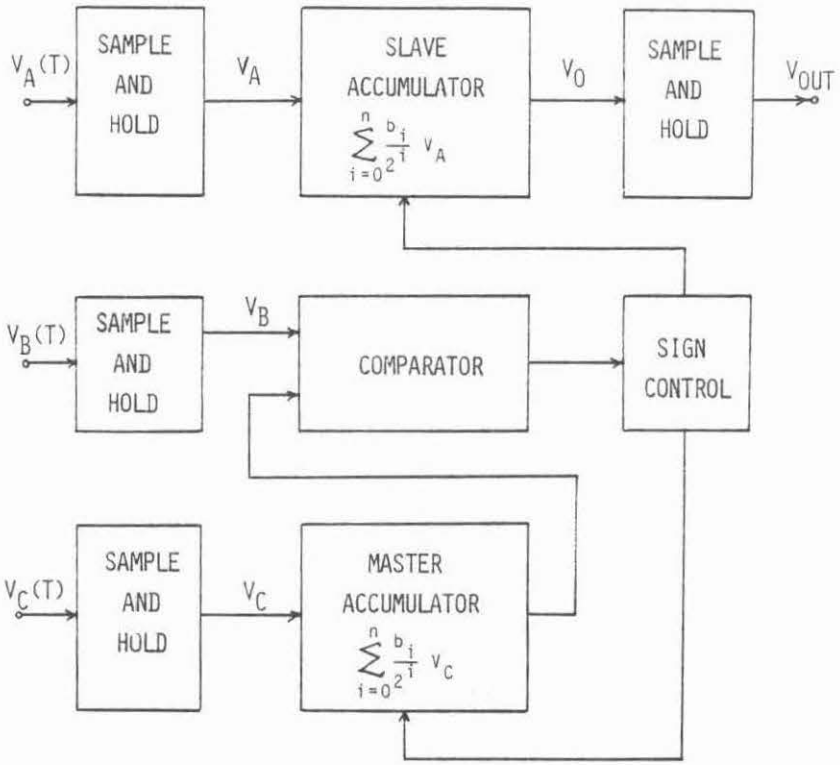


Fig. 5 - Block diagram of the successive approximation implementation.

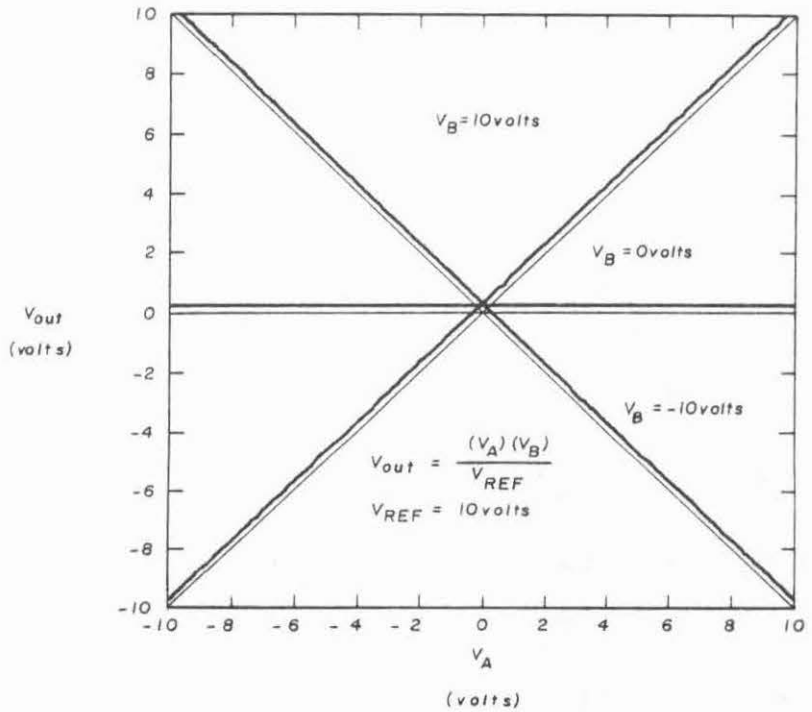


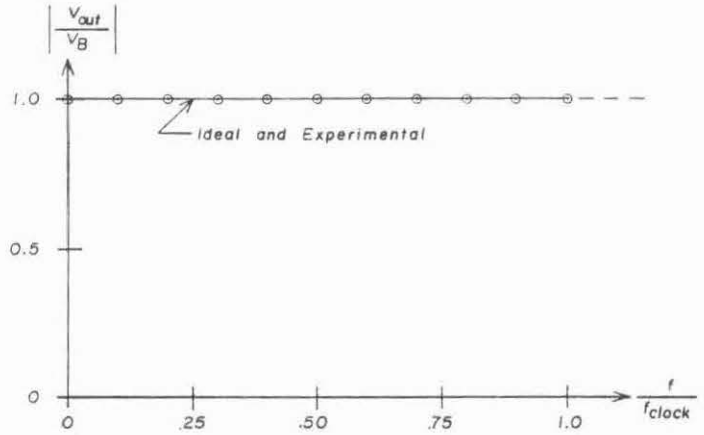
Fig. 6 - Experimental static characteristics of the multiplier. V_{OUT} versus V_A with V_B constant.

...tiply operation would be a constant.

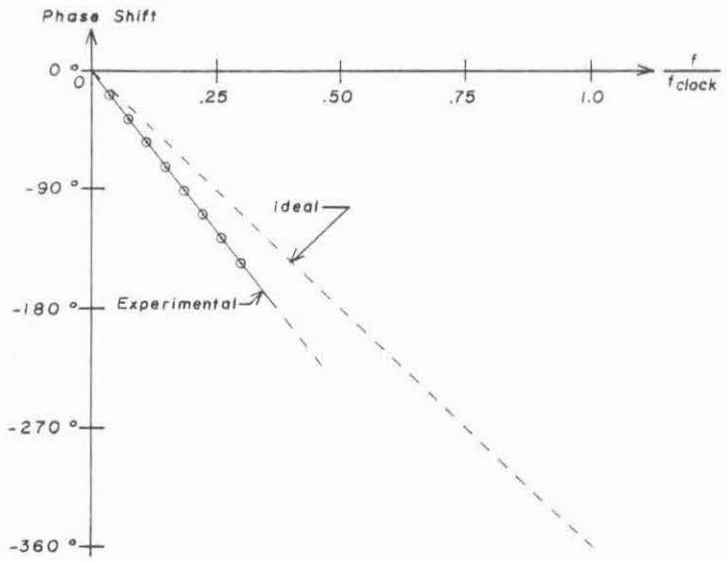
...ORMANCE

The static performance of a multiplier is typically characterized by offsets, feedthrough, and nonlinearities. Offset is due to an output voltage when both inputs are zero. Feedthrough is defined as an output when one of the inputs is zero and the other varies over its range of possible values. Nonlinearity has to do with the fact that the output of the multiplier may not be exactly equal to the product of the two inputs. The static performance of the breadboard version of the SC multiplier is shown in Fig. 6. To obtain these plots, V_C was connected to a +10 volt supply. V_A was set to -10, zero, and +10 volts to produce the three lines shown, and V_B was then swept over the range of -10 to +10 volts. As one can see, errors are mainly due to a constant offset of about 156 millivolts. This is a result of the number of successive approximations chosen for the breadboard version. Eight approximations are performed for each iteration. Since one approximation is discarded for resetting accumulators, seven useful approximations (n = 7) remain. If in this case, V_c = 10 volts, then the useful range of V is from -10 to +10 volts or 20 volts to ... s means that t... ximum error would then be $2V_c$ 20 volts ... or ... Because this ... or is constant as shown, it 2^n 2^7 can easily be nulled out by a single adjustment to be mentioned later. The results are similar when V_A is held constant and V_B is swept over its useful range.

In addition to these static characteristics, the bandwidth of the multiplier is also of interest. The bandwidth can be defined in terms of the magnitude response or the phase response. The best dynamic definition is the frequency at which a 1% absolute error is introduced in the multiplication operation. Figure 7 shows a plot of magnitude and phase versus frequency for a sine wave applied to the V_B input. The inputs V_A and V_C are each held at 10 volts. Note that the magni-



(a.) MAGNITUDE RESPONSE



(b.) PHASE RESPONSE

Fig. 7 - Frequency response of the SC multiplier. (a.) Magnitude and (b.) phase response.

tude remains constant regardless of frequency, and that the phase shift is a linear function of input frequency.

In the MOS version the offset error in Fig. 5 will become more important because of the clock feedthrough of the switches (not to be confused with the multiplier feedthrough). Because of the large clock signals and the possibility of high impedance states, small portions of the clock transitions will appear on the capacitors of Fig. 4. Although this feedthrough can become dependent upon the signal level, for purposes of this paper we shall assume that it is constant. Fortunately, in SC circuits we have the opportunity to sample the output offset and to introduce a cancelling component during the clock phases. To see how we can apply this idea to cancel the offset, let us consider the influence of the clock feedthrough. If the clock feedthrough introduces a constant component in the output, say ε, then we can write the output of the two accumulators at the end of a multiplication sequence as

$$V_{out} = K V_A + \varepsilon \tag{8}$$

and

$$V_B = K V_C + \tag{9}$$

where K is expressed as

$$K = \pm\frac{1}{2} \pm\frac{1}{4} \pm\frac{1}{8} \ldots \pm\frac{1}{2^n} \tag{10}$$

where n is the number of steps in the successive approximation of V_B of the multiplier. The approach taken to reduce this clock feedthrough is to build the dummy accumulator shown in Fig. 8. The dummy accumulator is identical to the other accumulators except that it has no input, and is not allowed to accumulate due to the discharge of the feedback capacitor C around the op amp during each clock cycle (this switch on the other two accumulators only operates once during the entire multiply sequence). In this manner a voltage will appear across

the two output capacitors which is caused by the clock feedthrough and the op amp offsets. These two capacitors will be applied on the same clock phase to the two accumulators in such a manner as to cancel the offsets due to the clock feedthrough and op amp offsets of these accumulators. If the dummy accumulator is matched to the actual accumulators, then the offsets should cancel. Furthermore, this system has the ability to track changes in the offset due to different clock amplitudes or temperature changes.

The nature of the operation of this multiplier prevents serious problems in multiplier feedthrough. If the A input is zero, then only clock feedthrough and op amp offset can contribute to an output but the dummy accumulator scheme of Fig. 8 should remove this output to minimize the B feedthrough. If the B input is zero, a_i should become close to zero since the dummy accumulator is removing the ε value in eq. (3).

Since the error caused by mismatching of the capacitors is constant and since we are assuming that the clock feedthrough is not a function of the input amplitudes, then the nonlinearity of the multiplier should be very small. The dynamic range of the multiplier should be limited only by the power supplies and the ability of the dummy accumulator scheme to cancel the offsets caused by clock feedthrough and op amp offsets. Indeed, breadboard results of the SC multiplier circuit show that non-linearities are almost negligible with matched accumulators. More extensive measurements are being conducted at present.

CONCLUSIONS

This paper considered the design of a SC multiplier which can be implemented using MOS technology. This circuit is compatible with other signal processing circuits designed by SC methods. The multiplier has four quadrant capability and has the potential of requiring no adjustments before application. The accuracy of the multiplier appears to very comparable to existing multipliers and the opportunity to use offset cancelling techniques give the promise of excellent static characteristics. The circuit requires 6 op amps and 11 capaci-

tors in its present form including the dummy accumulator. At present, portions of Fig. 5 are being implemented using MOS technology to further study the effects of clock feedthrough and other sources of error to the multiplier operation. The next step will be to integrate the entire circuit and to analyze the performance of the system and to study potential applications.

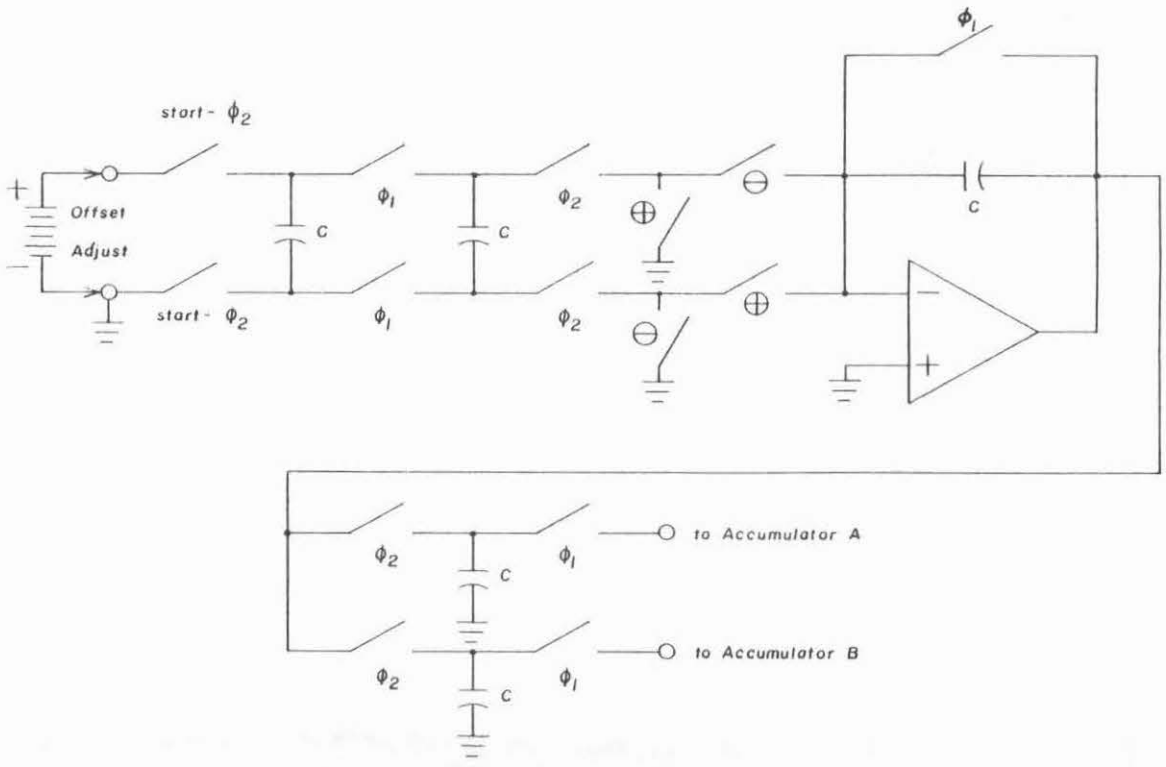


Fig. 8 - Dummy accumulator used to cancel offset.

REFERENCES

1. D.A. Hodges, P.R. Gray, and R.W. Brodersen, "Potential of MOS Technologies for Analog Integrated Circuits", IEEE J. of Solid-State Circuits, Vol. SC-13, No. 3, June 1978, pp. 285-294.
2. J.L. McCreary and P.R. Gray, "All-MOS Charge Redistribution Analog-to-Digital Conversion Techniques - Part I", IEEE J. of Solid-State Circuits, Vol. SC-10, No. 6, pp. 371-379, Dec. 1975.
3. R.W. Brodersen, P.R. Gray, and D.A. Hodges, "MOS Switched-Capacitor Filters", Proceedings of the IEEE, Vol. 67, No. 1, pp. 61-75, Jan. 1979.
4. T.R. Viswanathan, K. Singhal, and G. Metzker, "Application of Switched Capacitor Resistors in RC Oscillators", Electronic Letters, Sept. 28, 1978, Vol. 14, No. 20, pp. 659-660.
5. B.J. Hosticka and G.S. Moschytz, "Practical Design of Switched-Capacitor Networks for Integrated Circuit Implementation", Electronic Circuits and Systems, March 1979, Vol. 3, No. 2, pp. 76-88.
6. Y.S. Lee, L.M. Terman and L.G. Heller, "A Two-Stage Weighted Capacitor Network for D/A - A/D Conversion", IEEE J. of Solid-State Circuits, Vol. SC-14, No. 4, August 1979, pp. 778-781.
7. K.B. Ohri and M.J. Callahan, Jr., "Integrated PCM Coder", IEEE J. of Solid-State Circuits, Vol. SC-14, No. 1, Feb. 1979, pp. 38-46.
8. A.R. Hamade, "A Single Chip All-MOS 8-Bit A/D Converter", IEEE J. of Solid-State Circuits, Vol. SC-13, No. 6, Dec. 1978, pp. 785-791.
9. B. Fotouki and D.A. Hodges, "High-Resolution A/D Conversion in MOS/LSI", IEEE J. of Solid-State Circuits, Vol. SC-14, No. 6, Dec. 1979, pp. 920-926.
10. J. Bingham, "SC Modulators", Switched-Capacitor Workshop, Feb. 10-12, 1980, Palo Alto, CA.
11. B.A. Gilbert, "A Precise Four-Quadrant Multiplier with Subnanosecond Response", IEEE Journal of Solid-State Circuits, Vol. SC-3, No. 4, Dec. 1968, pp. 365-373.
12. K. Martin and A.S. Sedra, "Stray-insensitive Switched-capacitor Filters Based on Bilinear Z-Transform", Electronics Letters, Vol. 15, No. 13, June 21, 1979, pp. 365-366.